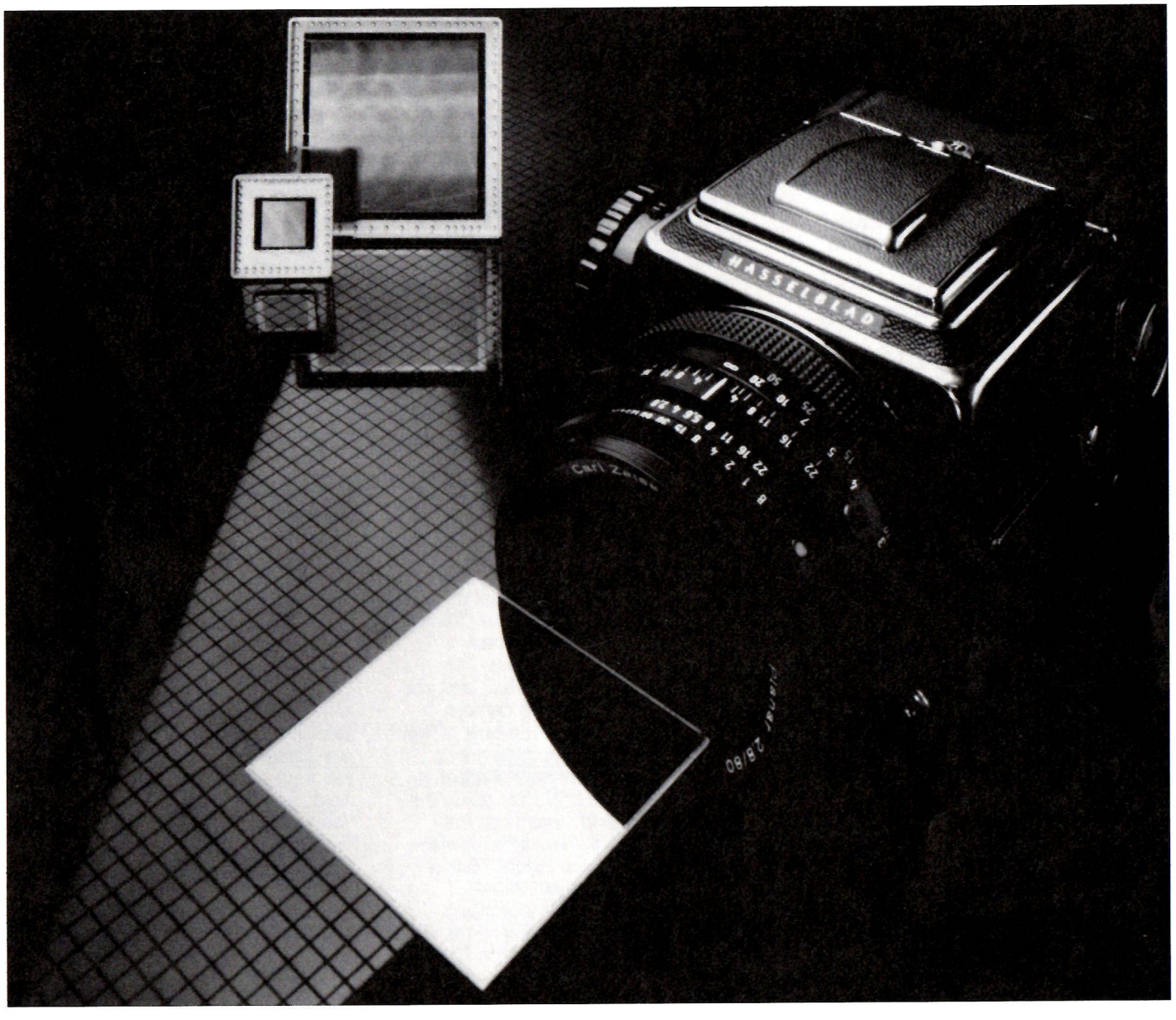
AN INTRODUCTION TO THE IMAGING CCD ARRAY



Tektronix®
COMMITTED TO EXCELLENCE

An Introduction to the Imaging CCD Array

The Tektronix TK512M and TK2048M Integrated Circuits are Charge-Coupled Devices designed especially for imaging applications and may be regarded as a piece of "electronic film." A sensitive, high resolution electronic camera is formed by combining the CCD with a suitable lens system, cooling equipment, and electronic circuits. The cameras find wide application in a variety of scientific, machine vision, and medical imaging areas.

The Tektronix CCDs, representing years of process development and design experience, offer excellent sensitivity, resolution, and a dynamic range of over 80 dB. This performance is realized only with carefully designed support circuitry. The critical requirements are perhaps better appreciated when we note that the lowest CCD signals detected correspond to less than ten electrons.

This note presents some basic concepts describing charge coupled devices. Some special techniques and terms unique to Tektronix CCDs are then presented. Finally, some of the special circuits for CCD operation are discussed.

CCD Fundamentals

The examination of the CCD begins with a discussion of the device concepts. Emphasis is on simple models. The bibliography contains references with more detailed information. The first structure considered is the surface channel CCD, simpler than the buried channel device to be described later.

The structure begins with a wafer of p-type silicon. A thin insulating layer of silicon dioxide is grown on the wafer surface. A thin metal film is then evaporated on the insulator in a pattern to form a small MOS (Metal-Oxide-Silicon) capacitor. See Figure 1A. The metal thickness is small, allowing light to pass through the film with minimum attenuation.

A positive potential is applied to the metal film, or gate, with the semiconductor bulk as the ground reference. The applied bias will sweep holes away from the gate to create a depletion region, a volume with no mobile carriers.

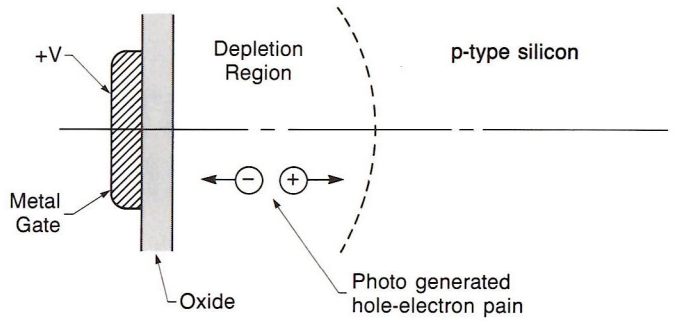


Figure 1A

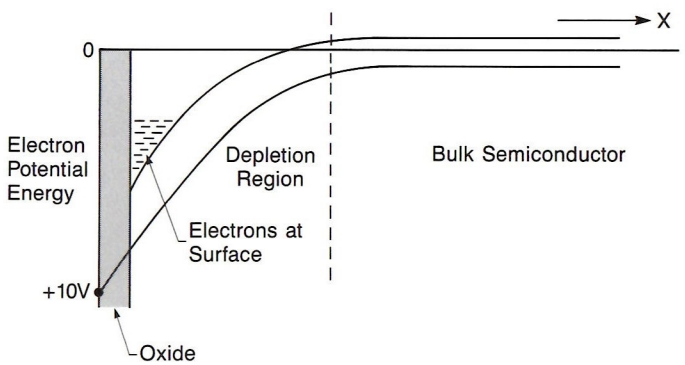


Figure 1B

The device is now illuminated. Light passes through the transparent metal electrode into the bulk material. Some of the incident light is absorbed, generating hole-electron pairs. The electric fields from the applied bias act upon the newly generated carriers, sweeping the holes into the bulk of the semiconductor. The electrons are urged toward the positively charged gates, and migrate until they reach the silicon-silicon dioxide interface. The electrons remain at this interior surface of the MOS capacitor. Figure 1B is a potential energy diagram for an electron within the fields described. The two lines shown represent the conduction and valence bands. The quasi-Fermi level for holes coincides with the zero potential.

The diagram of Figure 1B shows the variation in potential directly under a gate electrode, along the center line of Figure 1A. Electric field components parallel to the surface appear as we move away from the center. These fields confine the charge to the volume under the gates. If these fields were not present, the charge would diffuse away from the gate region. Charge confinement fields can arise in other ways. For example, a diffusion layer (here, a heavily p-doped region) will create junction-like effects. The resulting bound charge produces a field to inhibit charge motion across the p p+ interface. This creates a "channel stop," thus constraining the paths where charge may travel.

Consider now a more interesting structure, one capable of imaging. A linear array of closely spaced polysilicon gates replaces the single metal gate. Polysilicon takes the place of a metal film because it is transparent. Further, polysilicon may be formed with chemical vapor deposition, the "main stream technology" used for fabrication of most modern semiconductor devices.

Copyright©1987, Tektronix, Inc. All rights reserved.

Viewing the device surface, the polysilicon gates form an array of horizontal lines. A vertical channel is defined by the diffused channel-stops described above. (There will eventually be many vertical channels, but only one is considered now.) The area formed by three adjacent horizontal polysilicon lines and two diffused vertical channel stops defines a single sensing region called a picture element, or pixel. The significance of three gates per pixel will become apparent later.

One gate in the line-array has a positive voltage with the others grounded. Illumination strikes the array, creating hole electron pairs. Those electrons created within, or close to the depleted part of a channel (under the positively biased gate) collect under the positive gate. Charge accumulates during the time interval when light is present, termed the "integration period." The charge accumulated is the time-integrated result of light hitting the region during that period. Although carriers created in the field-free regions (under grounded gates) are not urged in any particular direction, they will still diffuse throughout the structure. Some enter regions under a positively biased gate where they contribute to the collected charge.

The photoelectric process described above is the major source of charge carriers in a CCD. Hole-electron pairs also arise from thermal carrier generation. While the photo electrons are desired, the thermally generated carriers represent an undesired noise, a "dark current." Cooling will reduce thermal carrier generation.

The integration period ends with a shutter closure, or by otherwise terminating the illumination incident at the CCD. The captured charge may be stored for extended periods with little attenuation. The only charge that continues to accumulate is the thermally generated dark current.

The charge generated by the impinging photons collects in potential wells, or "buckets." The charge is proportional to the number of incident photons arriving at each pixel during the integration period with the total determined by the light intensity (photons per second), integration time, and conversion efficiency. The user determines the first two parameters.

The final parameter, the quantum efficiency (QE), is a function of the CCD material and design. High QE produces high sensitivity in low light level applications.

The charge generated by photoionization is stored under positively biased CCD gates. The charge only becomes useful when it can be moved through the array and eventually measured. To achieve this, a gate adjacent to the charge storing element is positively biased. Previously confined electronic charge is now free to diffuse and reside under one of two adjacent gates. Having spread the charge between two elements, the bias on the first is dropped to zero while keeping the second positive. The charge originally under one gate has been transferred to an adjacent one. The process repeats to move the charge down the line of gates. Charge is eventually measured at the CCD edge.

The conceptually simple structure described is actually very complex; it requires one wire for each gate. Further, only one element collects charge at a time. A practical device results if the simple array is replaced with a periodic three-phase structure.

A pixel (picture element) consists of three gates. Positive gate ($\phi 1$) is followed by two more operating at zero bias during integration, "$\phi 2$" and "$\phi 3$." The structure is periodic along the surface with all "phase 1" gates attached to a common bus wire, and so on. The new structure requires only three wires leading to the outside world.

Illumination strikes the entire linear array during the integration period causing charge to collect under every third gate. Then, voltages applied to the three phases cause the electrons to move along the array. Figure 2 shows the timing signals and a schematic sketch of the transfer process. The clock signals overlap in time. A charge residing under one gate moves to the next only when a common, larger depletion region exists.

The periodic structure is a more efficient collector of photo electrons. Those carriers generated under zero bias gates are still close to gates with a positive bias. They will diffuse to the positive gates where they are confined by the fields of the potential well.

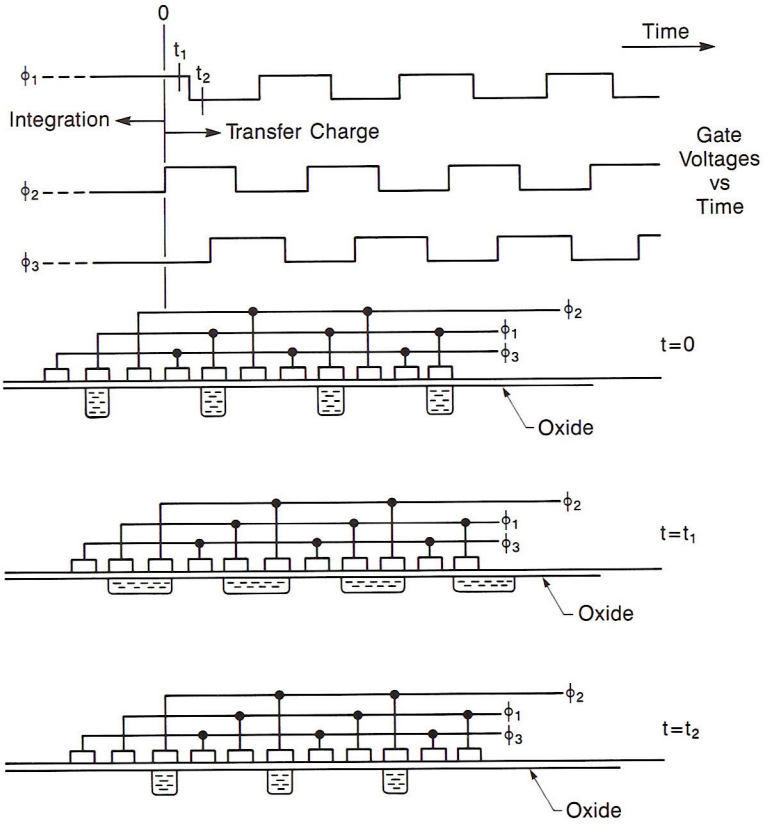


Figure 2

A literature review reveals CCDs with a wide variety of gate and oxide insulator structures. Some use a stepped oxide, with one gate phase having a different oxide thickness than an adjacent one. This produces an electric field with a horizontal component over part of each pixel. The charge transfer now requires only a two phase clock with efficient transfer in only one direction. The three phase structures effectively transfer charge in either direction.

The Buried Channel CCD

The design described above stores the charge at an interface between silicon and a thin, insulating layer of silicon dioxide. The stored charge must move along the surfaces during the transfer process. Semiconductor surfaces are often characterized by noise problems, frequently related to defects in the integrity of the surface. For example, the low frequency noise performance of junction FETs is usually better than that of otherwise similar MOSFETs. The drain-source channel of a JFET is within the bulk of a semiconductor and not at a surface.

Tektronix CCDs use a structure termed a "buried channel," created by ion implantation. Dopants driven through the oxide form an n-type layer a few hundred Angstroms below the semiconductor surface. Positive bias on this n-region forms a reverse biased diode with the bulk p material. It is at this junction that photo electrons collect. The n-layer is so thin that charge motion is still controlled by the potential of the gates above. The dark current is reduced significantly by elimination of charge at a semiconductor surface. Moreover, the charge transfer efficiency (CTE) is enhanced because the charge is now further removed from the conducting gate surface. This allows the potential of adjacent gates to be more significant in establishing the local electric field.

The Tektronix Imaging Array CCD

The structure described above used a single channel, with a periodic array of gates. Multiple channels are desirable, allowing a large area to function as a photodetector. Present Tektronix CCDs are large area arrays segmented into three registers, termed A, B, and C. A separate three phase timing signal clocks each register.

Section B occupies the majority of the IC area. This is a collection of parallel diffused vertical channels. The gates driving these channels are long enough to encompass the entire array. Hence, the TK512M (**) will contain 512 vertical channels, intersected by 3 × 512 horizontal gate lines. The array is shown schematically in Figure 3. One cycle (pixel time period) will transfer the charge in each of the 512 channels upward or downward by one pixel distance. Each pixel has a dimension of 27 by 27 microns.

Our use of the terms vertical, top, and bottom refer to the sketches. There is no relationship to variations through the depth of a FET, as used in the term Vertical MOSFET (VMOS).

End register "A" is at the top of the integrated circuit, while register "C" is at the bottom. Registers A and C are 562 pixel serial arrays. Either register A or C will generate an output electrical signal. In contrast, the B register is a large (512 × 512 pixel) array with no direct output. One full cycle of the "B" clock will transfer charge through the array to load an end register with a line of signals. The resulting data line may then be transferred to the readout electronics at the end of the register, one pixel at a time. A total of 562 complete "A" clock cycles (rather than 512 cycles) occur for each cycle of the "B" register. The extra 50 cycles, discussed later, serve a calibration function.

The B Register channels end in elements called transfer gates, labeled TA or TC. These serve an isolation function. TA is positive during the entire period when a parallel pixel group is being transferred from the B to the A register. The transfer gate then switches to a low state. This isolates the charge moving along the A register from that stored in the B register. (A slight negative bias on TA may provide further isolation.)

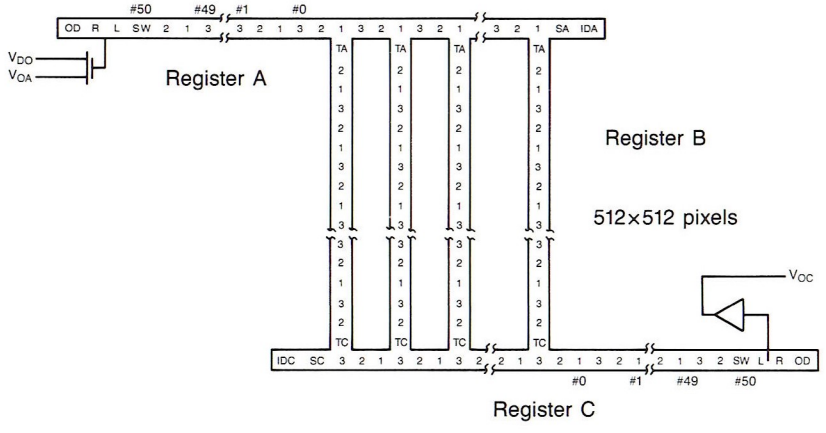


Figure 3

** The text refers to the TK512M, with the understanding that the same concepts describe the TK2048M, which contains 2048 × 2048 pixels in the B register. Capacitance differences are the most significant. As N increases, the capacitance of the end registers will increase linearly. The capacitance of the imaging register, B, will increase according to N-squared.

Registers A and C are identical. Each is 562 pixels long, with each pixel defined by 3 gates. The A and C pixels are twice the size of those in the B register.

Each end register begins with an input diode, IDA or IDC, followed by a sample gate, ϕ-SA or ϕ-SC. These allow the electrical injection of charge into the end register. The charge may then be shifted into the B register. This allows the array to be biased with a predetermined charge per pixel before illumination and integration. The resulting uniform charge background is called a "fat zero." Charge is not injected during typical operation. Sensitive scientific applications for which the Tektronix CCDs were designed rarely use the fat zero technique.

Registers A and C end in oversized gates called summing wells. Additional gates for control and buffering, a low capacitance isolated diffusion, and an output amplifier conclude the structure at the end of the readout registers. Details are presented in a later section.

The end registers are longer than the required 512 pixel minimum by 50 pixels. The extra pixels do not receive charge from the B register. They calibrate the camera, for they represent pixels without illumination.

Tektronix builds CCDs for either front or back illumination. Front illumination (through the polysilicon gate electrodes) is appropriate for longer wavelengths, approaching the infrared spectrum. These lower energy photons have a large penetration depth. As such, they must travel through a substantial semiconductor volume before absorption.

Higher energy photons (visible, ultraviolet, x-rays, and even electrons) are absorbed with great ease in silicon. If allowed to impinge upon the CCD front side, the carriers may be created in the gates or oxide layers, before the photon reaches the semiconductor bulk. Efficiency is significantly improved by turning the CCD over and illuminating the back of the array. However, the array thickness must be reduced to realize good quantum efficiency. The thinned, backside illuminated CCDs are only ten microns thick and are, understandably, more difficult to build.

Pulse Generation and Driver Circuits

The previous discussion detailed the way charge moves in a CCD as voltages are applied. The multiphase structures used cause many gate voltages to change with a single terminal voltage. For example, the TK512M has a total of 262,144 pixels in the B register. The total charge stored in that register is moved by pulsing only three electrodes at the edge of the integrated circuit. One row of charge (512 pixels) may be transferred to an end register (A or C) by pulsing the appropriate transfer gate. The charge that then resides in an end register may be read by a serial transfer. Pulses applied to the A (or C) gates cause the row of charge to move to the register end where it is detected.

The waveforms required by the CCD are generally rectangular in time. The circuitry that generates these voltages is segmented into two categories, the timing circuits (logic) and the wave shaping (driver) circuits.

All of the circuits that follow are ones that have been used in some of the Tektronix test cameras.

A variety of digital methods have been used. The timing system should feature experimental flexibility. A test camera clock system might begin with a chain of digital dividers or a long shift register. Decoded output states set or reset R-S Flip-flops. This system is easily programmed, usually with wiring, to accommodate a new device or clock speed. An etched circuit, if used, should provide this flexibility. Application-specific digital circuits, such as a PAL, are best left for production applications.

Pulse generation in our test cameras used TTL, LS-TTL, CMOS, and some of the new, higher speed families including high speed CMOS. The high power supply current pulses of some logic families (TTL) sometimes generate digital noise. This is often difficult to eliminate from low noise amplifier outputs. This problem is often reduced with ECL circuits; faster circuits are not always noisier.

A computer is a central part of a scientific CCD camera. The analog CCD output will eventually be converted to a digital word with an analog to digital converter. The word is then processed by a computer for assembly into images. The computer software may even include signal processing.

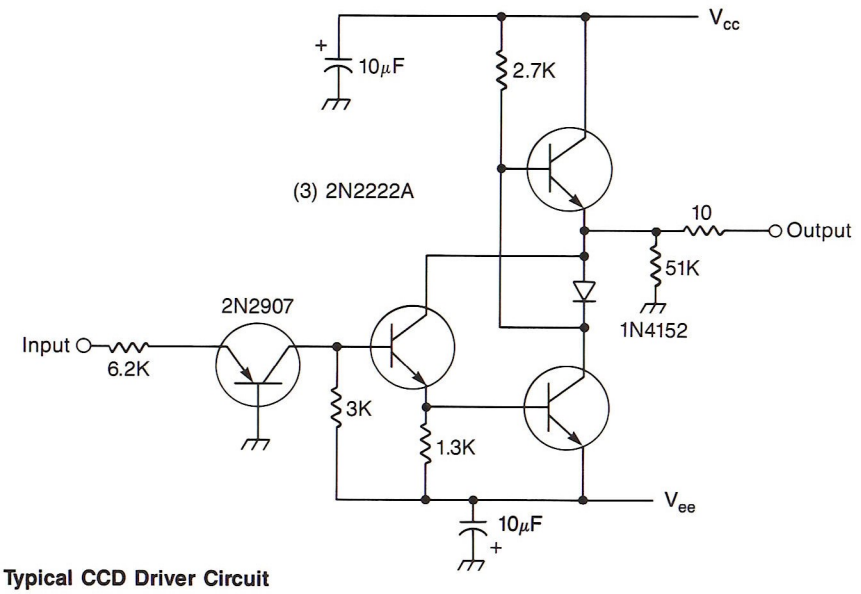
It is tempting to use the computer for the direct generation of clock pulses. Unfortunately, this has not worked well because the CCD requires very low timing jitter. This is best provided by a periodic digital pulse generator derived from a stable source. A crystal controlled master clock is preferred for most applications. Some slow timing and control functions may use the computer. An example is the timing of a shutter. A computer could even be used to control a programmable, stable timing chain. This would retain the flexibility of software timing while providing the stability needed for low noise CCD operation.

A driver circuit must condition the logic signals before application to the CCD. The upper and lower pulse voltages must both be well defined, with low noise and minimal overshoot during a transition. Voltage transitions are modest, typically 10 to 15 volts. The most difficult requirement for a CCD driver is the ability to charge large capacitors.

The estimated CCD capacitances differ for the various array registers, and are listed below:

Electrode	TK512M	TK2048M
A or C Gate	150 pF.	600 pF.
B Gate	7500 pF.	0.13 μF.
Reset Line	5 pF.	5 pF.
Transfer Gates	300 pF.	1200 pF.

Figure 4 shows one popular CCD driver circuit. A common base PNP input stage isolates the driver output from the digital input while shifting the dc level. The pseudo complimentary output provides high current capability. This circuit has a restricted rise time, owing to the low base current available to the upper (NPN) output transistor. Fall time is less restricted. Output voltages are set by adjusting V-cc and V-ee. This amplifier shows a transient response that depends upon the V-ee level, a major deficiency.



Typical CCD Driver Circuit

The input is driven with a logic signal (CMOS, TTL, etc.) The higher positive output level is set by adjustment of V-cc. the lower output voltage is controlled by V-ee. Typical levels are V-cc = +8 and V-ee = −2 volts. V-ee must be more negative than −0.8 volts for the circuit to function.

Figure 4

Figure 5 shows two useful and simple driver circuits. That in Figure 5A uses a CD-4049 inverter. This integrated circuit includes internal protection that allows an input voltage higher than the positive supply voltage. As such, it is useful as a level shifting element. Paralleling inverters from the six available in the package increases the available output current.

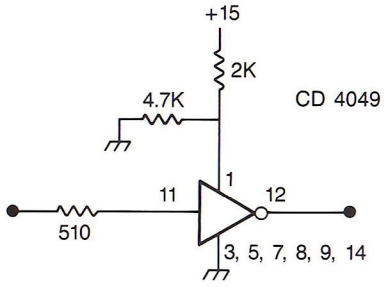


Figure 5A

Figure 5B shows a dual driver circuit. The integrated circuit is the DS-0026, a MOS memory/clock driver. This circuit is convenient where several CCD electrodes must receive the same clock voltages. However, the only method to control the output level is power supply adjustment. The RC output networks control the rise and fall time. An asymmetrical transient response may be generated with a diode-resistor network paralleling the 20 ohm output resistor shown. Considerable power supply decoupling is recommended for use with this circuit.

Additional commercially available circuits qualify as CCD drivers. These include the DS-0056 MOS clock driver, DG-100 and DG-200 series analog switches, and LM-0002 current booster.

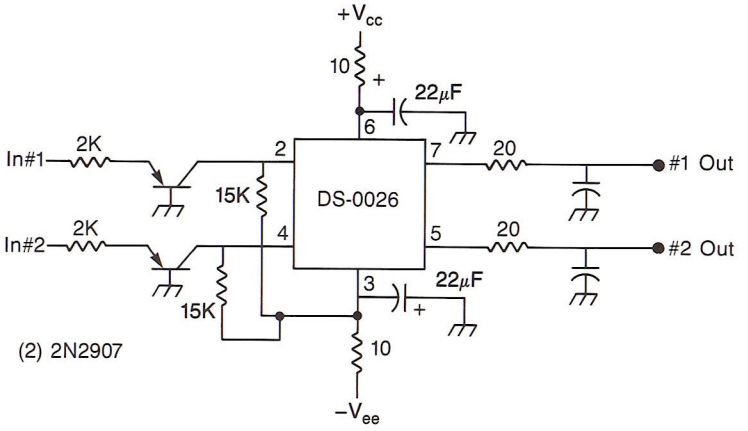


Figure 5B

The load capacitance, mentioned earlier, can be very high. This must be considered when picking transistors and designing decoupling networks. Some circuits suffer from poor stability when driving a capacitive load. Hence, Darlington amplifiers should not be used in these applications. The drivers should be unilateral to prevent stray output transients from appearing on the driver input.

Output Signal Readout and Correlated Double Sampling

The A and C registers terminate in a structure that provides an electrical readout of the CCD charge. The structure consists of the summing well, a "last gate," a small capacitor, a switching MOSFET, and an output MOSFET amplifier. These elements function collectively to transfer the charge of a single pixel to the small capacitor. The capacitor is attached to the gate of a MOSFET amplifier, with an output voltage proportional to the pixel charge.

The critical capacitor used for charge measurement is called the floating diffusion. This element is part of the thin ion implanted n-type layer below the gate oxide. The small portion of this layer used to read output charge is isolated from the rest of the layer by a biased gate. As the name implies, the capacitor floats in potential, without a dc attachment to other CCD elements. Before reading the charge in each pixel, the capacitor potential is set to a well defined voltage with a MOSFET switch. The switch is referenced to an external CCD terminal, labeled ODA or ODC in Tektronix CCDs.

A readout sequence begins with the reset pulse, setting the initial capacitor voltage to ODA with the FET switch. The switch is then opened, isolating the capacitor. There is a small shift in the capacitor voltage as the reset pulse ends, the result of capacitive coupling across the FET switch. Once the capacitor has been reset, CCD charge transfers to the capacitor, altering the voltage. The charge is usually that associated with but one CCD pixel.

The on-chip amplifier is a source follower. Hence, the source voltage is a measure of the charge on the capacitor. This can be a very difficult measurement owing to the low signal levels. Recall that CCD charges are as low as 10 electrons. A typical CCD output sensitivity is 0.6 microvolt per electron.

An oscilloscope would show the FET source waveform of Figure 6. The cycle begins with the reset FET (a). A large pulse may occur, the result of capacitive coupling through the FET and the history of charge from the past cycle. The charge eventually disappears (b) with the capacitor reaching the reset potential, ODA. Pulses now begin in other parts of the CCD, producing small feedthrough components (c). The charge from the last pixel begins to flow onto the output capacitor, (d), reaching the final potential (e). The voltage at (e) will depend upon the number of photoelectrons created in the addressed pixel during the integration period.

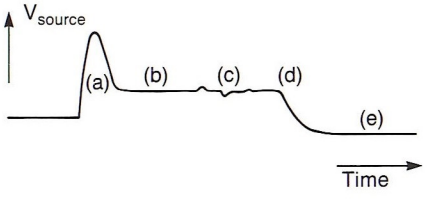


Figure 6

The signal voltages are quite small and are often buried in noise. Although digital feedthrough is usually dominant, the main natural noise source, and the ultimate limitation, is the thermal noise in the resistance of the FET reset switch. This is often termed kTC noise with a typical value corresponding to 100 to 300 electrons, rms.

The kTC noise, and much of the digital feedthrough noise are eliminated with a technique called Correlated Double Sampling (CDS), a slight modification of the sequence just described. The process again begins by resetting the on-chip sampling capacitor. Shortly after the reset pulse has ended, but BEFORE transferring any CCD signal charge, the follower output voltage is sampled and remembered in an off-chip capacitor. CCD charge transfer then occurs, altering the voltage of the on-chip sampling capacitor. The new result is again sampled and remembered. The two samples differ only by a voltage corresponding to the transferred charge. Results from the first and second samples are subtracted in an analog circuit with the difference applied to the output for eventual conversion to digital form.

The kTC noise has been eliminated by the subtraction. The output signal is the result of a difference between two signals that each contained the information related to the resistor noise. The noise at the time of the second sampling pulse was unchanged from the instant of the first sample. The two noise components were correlated in time. Thus the difference signal is contaminated only by the uncorrelated noise of the on-chip output MOSFET amplifier. The Tektronix amplifier is specified for a low maximum noise of only 10 electrons, RMS.

The signals extracted from the CCD are analog voltages. They are sampled, with results temporarily stored in a capacitor, and even processed (subtracted.) Still, they remain as purely analog signals throughout most of the signal chain. An analog to digital conversion occurs at the end of the CDS system. Further processing of the digitized data may, of course, occur in the computer.

The video system in a Tektronix test camera illustrates many of the concepts with the circuitry serving a multiplicity of functions, including CDS. The system begins with the on-chip, "floating diffusion" sampling capacitor. This has a very small capacitance value, about 0.5 pF. The capacitor attaches to the gate of the on-chip source follower amplifier.

The chip output is immediately increased with the preamplifier shown in Figure 7. This is a non-inverting amplifier with a typical voltage gain of 20 to 25.

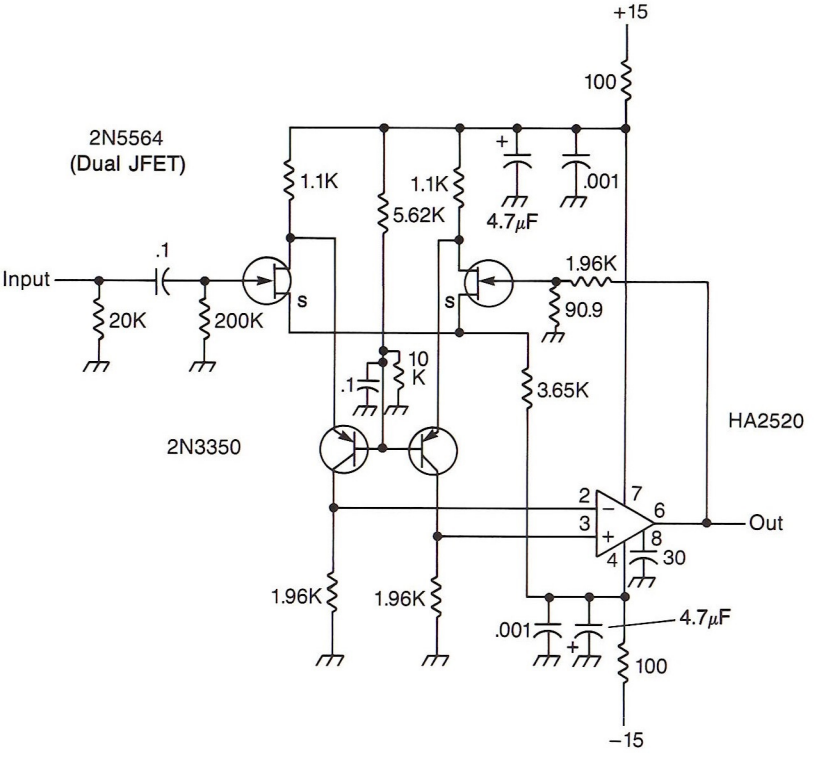


Figure 7

The preamplifier input impedance is dominated by the the 20K load resistor (Figure 7.) This value must be moderately high owing to the high output resistance of the on-chip source follower. The on-chip FET is a small area device, required for low gate capacitance. However, the small FET area yields a low transconductance, (typically 0.0001 S) producing an on-chip amplifier with less than unity gain and a high output resistance.

The preamp drives a circuit board containing the rest of the signal processing circuitry, presented in Figure 8. The first stage, the "postamp," is an op-amp with an inverting gain of about 12. The output is a.c. coupled via a 470 pF capacitor to the "Clamp Buffer," a unity gain circuit with very high input impedance. The input may be shunted to ground with a CMOS 4053B Analog switch. The buffer output then goes to a sample-and-hold circuit.

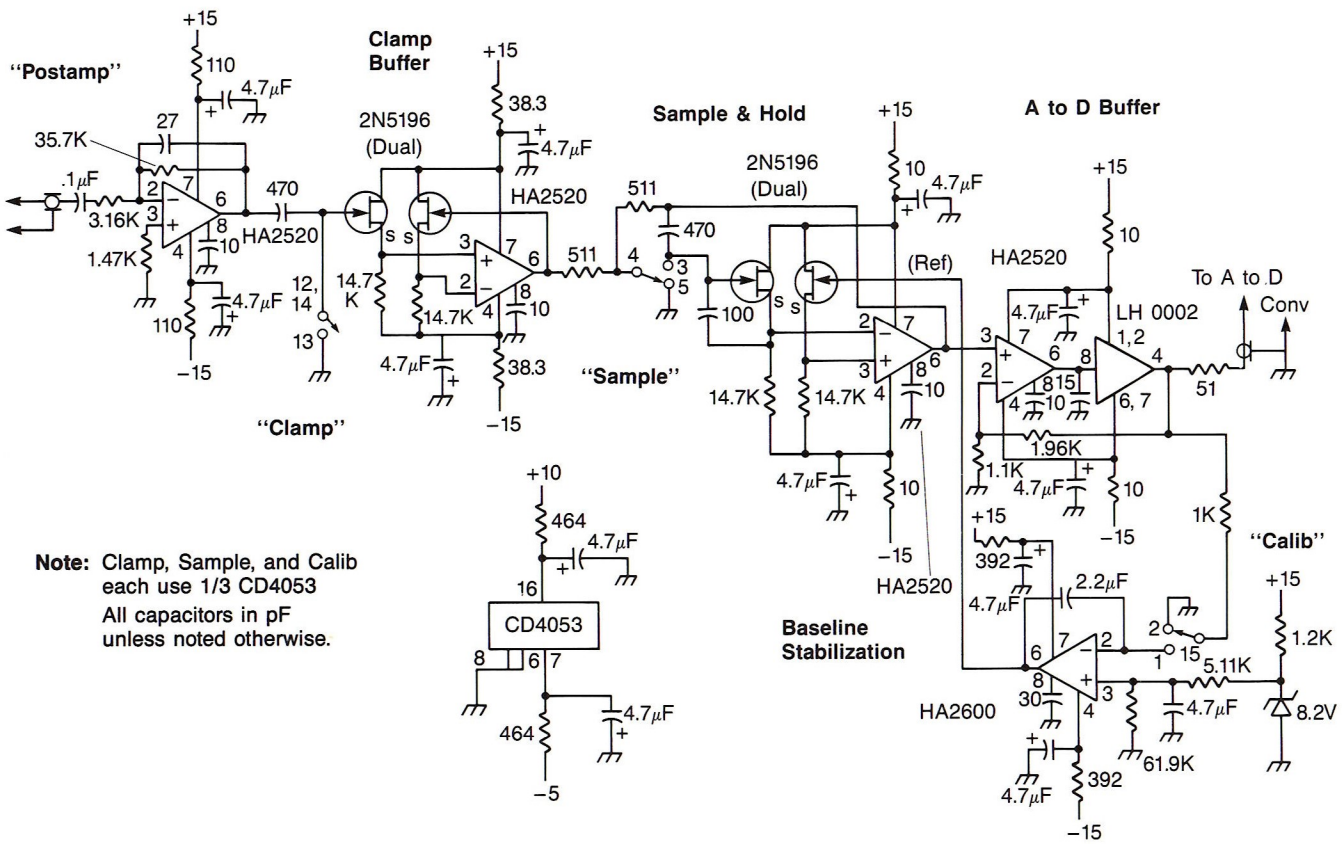
The final stage is a non-inverting amplifier with voltage gain just under 2. A 50 ohm output drives a suitable A-to-D converter. A second output drives a very slow integrator (1K ohm and 2.2 microfarad) through an analog switch.

The integrator is fed back to the non-inverting input of the sample-hold to provide a dc reference.

The test camera usually uses a 16 bit A-to-D converter with an 8 microsecond conversion time, the Intech A856-16. Some test cameras use the Burr Brown ADC-76 (16 bits in 17 microseconds) or ADC-803BM (12 bits in 1.5 microseconds.)

The operation of the system of Figure 8 is explained with the timing diagram shown in Figure 9. The sequence illustrates the correlated double sampling concept. However, the sequence used in practice may vary slightly.

1. The CCD is reset, defining the beginning of the pixel readout period.
2. There is a large feedthrough component from the reset pulse. This takes a long time to stabilize. Hence, there is a considerable delay between the end of the reset pulse and the first sampling. The postamp output is an inverted form of the waveform shown in Figure 9.
3. The postamp output signal contains the kTC noise information. The clamp pulse is now applied, shorting one side of the series 470 pF capacitor to ground. The voltage on the ungrounded side of the clamp capacitor remains stable, leaving the noise sample stored in the capacitor.
4. The clamp pulse ends. The voltage applied to the clamp buffer is now free to change. The final charge transfer on the CCD begins, controlled by the sample pulse of Figure 9. This coincides with the end of the clamp pulse. The sample-hold circuit also begins. The flow of charge in the CCD changes the voltage at the input to the clamp buffer and following stages. The subtraction eliminating the kTC noise component occurs in the series 470 pF capacitor.
5. The Sample pulse ends after most of the signal charge has been transferred to the CCD floating diffusion. The other circuits have followed these changes.
6. The sample-hold circuit turns off at this instant. The output is a stored sample of the output data just processed. It remains long enough for the subsequent analog-to-digital converter to function.



Note: Clamp, Sample, and Calib each use 1/3 CD4053
All capacitors in pF unless noted otherwise.

Figure 8

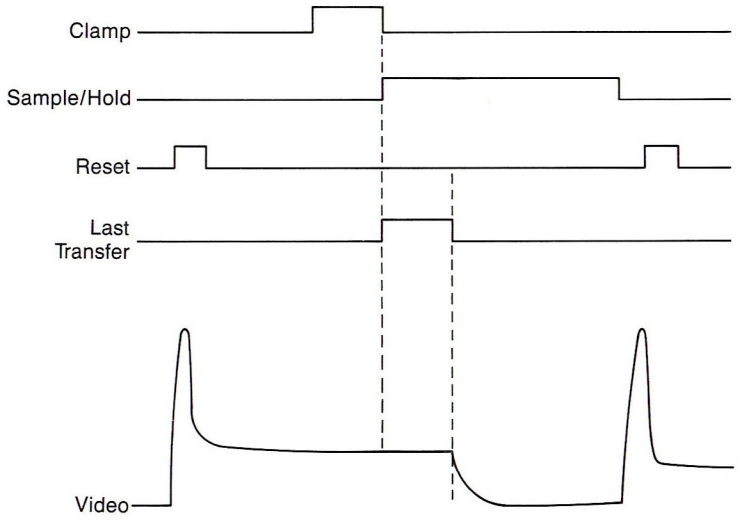


Figure 9

7. The slow integrator labeled "baseline stabilization" is a memory that indicates the dark status. Recall that each horizontal CCD register (A and C) has an extra 50 cells. The analog switch driving the integrator is on during the period when the dark bits are being read. This establishes the reference for the sample-hold circuit at a well defined "dark level."

An alternative to the system just described uses dual slope integration to perform the correlated double sampling. A reset pulse initializes the on-chip capacitor voltage. The result drives an integrator that charges a capacitor for a finite time period. Charge transfer then occurs, followed by integration for the same length of time, but with an inverted sense. The noise contaminated portion of the signal disappears, leaving only the difference, a representation of the information transferred onto the CCD output capacitor.

The exact duration and shape of the pulses used for CDS will vary with different systems. The reader is urged to study the references to gain appreciation for the more subtle details.

CCD Readout: On-Chip Details

CCD readout usually uses the correlated double sampling described in the previous paragraphs. The CCD uses special elements to enhance the charge measurement.

An enlarged charge storage region called the summing well occurs just before the final gate in a serial register (A or C.) Each serial pixel is twice the size of those in the parallel (B) register. The summing well is capable of charge storage twice that of other serial register pixels, or quadruple that of a parallel pixel. The summing well is sometimes used to store and collect the charge from up to four pixels at a time. Spatial resolution is reduced, but the signals are larger. Moreover, the output circuitry is now required to process less information. Hence, data bandwidth is less, offering the possibility of further signal-to-noise ratio enhancement.

The final gate in the Tektronix CCD is appropriately named the "last gate." It is usually dc biased and limits the amount of charge that may be stored in the summing well. Application of bias to the summing well defines the depth of the related potential well. This, in turn, limits the total charge that may be stored. The addition of negative charge cancels the effect of the positive bias, until the well is full. An intermediate bias applied to the last gate also alters the well capacity, allowing charge leakage once a partial capacity is reached.

A second function of the last gate is isolation. When biased to a low, but still positive potential, the last gate allows charge from the summing well to transfer to the output node capacitor. The gate with constant bias forms a shield, providing isolation between the pulsed gates in the register and the sensitive output node. The results are similar to the output-to-input isolation achieved in a cascode amplifier.

Figure 9 illustrates a subtlty: The transfer of charge to the output sensing capacitor follows the end of the "last transfer pulse." The reset pulse has already established the potential of the small output capacitor at a high value, with the "last gate" biased at an intermediate level. A positive summing well bias allows charge to diffuse into the summing well region. The lower voltage on the "last gate" establishes a field that inhibits current flow onto the last gate or the output capacitor. However, when the summing well returns to ground potential, diffussion into the "last gate" region is allowed, with subsequent flow into the deeper well (higher voltage) of the output readout capacitor.

Some Comments on Noise in CCD Systems

The full imaging capability of an array CCD is realized only when very low signal levels can be processed. The charges may be only that of a few electrons. Any noise can seriously limit system response.

Semiconductor noise may be segmented into several categories. Shot noise often dominates in a bipolar transistor and relates to the flow of current. Shot noise disappears when there is no current flow. The use of sampling methods, with special emphasis on the correlated double sampling, will remove much shot noise from the system output.

Shot noise related to gate leakage current can sometimes be significant in a FET. Low leakage specifications are, hence, important in a CCD.

Thermal noise is present in any resistor, even a piece of wire. The available noise voltage is proportional to the square root of the resistance. Hence, the voltage becomes more significant in the very high impedance systems used for CCD signal processing. The thermal noise voltage across the reset FET resistance was the critical noise element eliminated by correlated double sampling.

Flicker, or 1/f noise, often relates to the presence of traps associated with contamination and crystal defects. As such, it is semiconductor processing dependent. The buried channel process reduced noise related to surface defects in the CCD.

Amplifier noise performance is often specified by application of the noise figure and noise temperature concepts. These methods are not well adapted to a CCD system. The noise

figure concept concerns amplifier gain, and compares the output signal to noise ratio to that at the input. The viable power in these calculations is the "available power." Available power gain of a MOSFET video amplifier is not always well defined. Moreover, noise figure usually applies to a linear system with well defined bandwidths at each stage. The analog sampling process precludes linearity and confuses bandwidth issues.

Noise performance is often complicated by feedback. Negative feedback reduces the effect of a noise source within a loop. However, the trade-off in noise and gain performance can be subtle.

A more definitive analysis returns to fundamental noise modeling at the device level. The active devices are characterized by appropriate noise generators (voltage and current) within the device. The discussion in Gray and Meyer, Chapter 11, is outstanding in this regard.

The CCD on-chip amplifier is the first, and usually the most critical stage in the CCD system. Low noise here is vital. A low noise resistor should bias the on-chip follower. Although the amplifier shows available power gain, the voltage gain is less than unity, making the noise performance of the following stage critical to system performance.

Another type of noise in a CCD camera is differential across the array. That is, uniform light illumination across the camera lens (a "flat field") may not produce a uniform electrical output. These effects are best handled with software and system calibration.

Cooling the CCD

Dark current is often a major limitation to the minimum detectable optical signal of a CCD. Like most semiconductor leakage, dark current decreases (near room temperature) by a factor of 2 for each 8 degree C temperature decrease.

Liquid nitrogen (LN) cools the CCD in most low noise CCD cameras. The CCD is mounted in a zero insertion-force socket on the circuit board containing the drivers and low noise amplifiers. A hole in the socket places a copper block in intimate thermal contact with the non-illuminated side of the CCD. The copper element is cooled by LN and is warmed with a small heater. Closed loop temperature control is possible, if required.

The volume containing the cooled CCD and the critical circuitry is evacuated with a simple vacuum system to prevent convection warming and water vapor condensation. The equipment is always returned to room temperature before opening the vacuum system to the atmosphere. The vacuum system uses a small cryosorption pump.

The CCD will operate at room temperature. However, integration time and readout time must both be short to minimize dark current effects. A CCD operating temperature of −90 degrees C is usually cool enough to decrease the dark current below measurable limits. The Tektronix CCDs are specified for a dark current density of 10 nA per square cm at 25 degrees C. Operation at −90 degrees C allows one to integrate for over 1 hour with a typical dark current contribution of 1 electron per pixel.

A Peltier cooler is another option for temperature control. Some multistage coolers are available that will cool a CCD to 60 degrees C below ambient temperature.

The Tektronix CCD contains a temperature sensing resistor. Although not calibrated, this element displays the monotonic change of resistance with temperature required for closed loop control.

Acknowledgement

Although all of the circuits presented in this note have been used in Tektronix test cameras, many of the circuits were originally developed at the Jet Propulsion Laboratory of the California Institute of Technology. We gratefully acknowledge the contributions of these pioneers.

Bibliography

1. Boyle, W.S. and Smith, G.E., "Charge Coupled Semiconductor Devices," *Bell System Tech. Journal 49*, 587-593 (1970). Also see paper by the same authors in IEEE Spectrum, July, 1971.
2. Barbe, D.F., "Imaging Devices using the Charge Coupled Device Concept," *Prod. IEEE 63*, 38-67 (1975).
3. White, M.H., Lampe, D.R., Blaha, F.C., and Mack, I.A., "Characterization of Surface Channel CCD Image Arrays at Low Light Levels," *IEEE Journal of Solid-State Circuits*, Vol.SC-9, No. 1, pp 1-13, February 1974.
4. Hall, J.A., "Arrays and Charge-Coupled Devices," Chapter 8 of *Applied Optics and Optical Engineering*, Vol. VIII, Academic Press, 1980.
5. Gray, P.R., and Meyer, R.G., *Analysis and Design of Analog Integrated Circuits*, Second Edition, John Wiley & Sons, New York, 1984.
6. Janesick, J.R., Elliott, T., Collins, S., Marsh, H., Blouke, M.M., and Freeman, J., "The Future Scientific CCD," *Proc. S.P.I.E.*, 1984.
7. Blouke, M.M., Heidtmann, D.L., Corrie, B., Lust, M.L., and Janesick, J.R., "Large Area CCD Image Sensors for Scientific Applications," *Proc. S.P.I.E. Conference*, 1985.
8. Kosonocky, W.F. and Sauer, D.J., "The ABCs of CCDs," *Electronic Design*, Vol. 23, pp 58-63, April 12, 1975.
9. Bloyed, D., Lepaisant, J., and Varoquaux, E., "Very-low-noise amplifier for low-temperature pulsed NMR experiments," *Rev. Sci. Instrum. 56 (9)*, pp 1763-1771, September, 1985.

For further information, contact:
Charge-Coupled Devices
Integrated Circuits Operation
Tektronix, Inc.
P.O. Box 500
Mail Station 59-420
Beaverton, OR 97077
Phone:
(800) 262-4374 (outside Oregon)
(503) 627-2515 for technical assistance

Copyright © 1987, Tektronix, Inc. All rights reserved. Printed in U.S.A. Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX, TEK, PLOT 10, TEKTEST, SCOPE-MOBILE, and ® are registered trademarks. For further information, contact: Tektronix, Inc., Corporate Offices, P.O. Box 500, Beaverton, OR 97077. Phone: (503) 627-7111; TLX: 151754; TWX: (910) 467-8708. Subsidiaries and distributors worldwide.

Tektronix®
COMMITTED TO EXCELLENCE

2/87 82W-4022