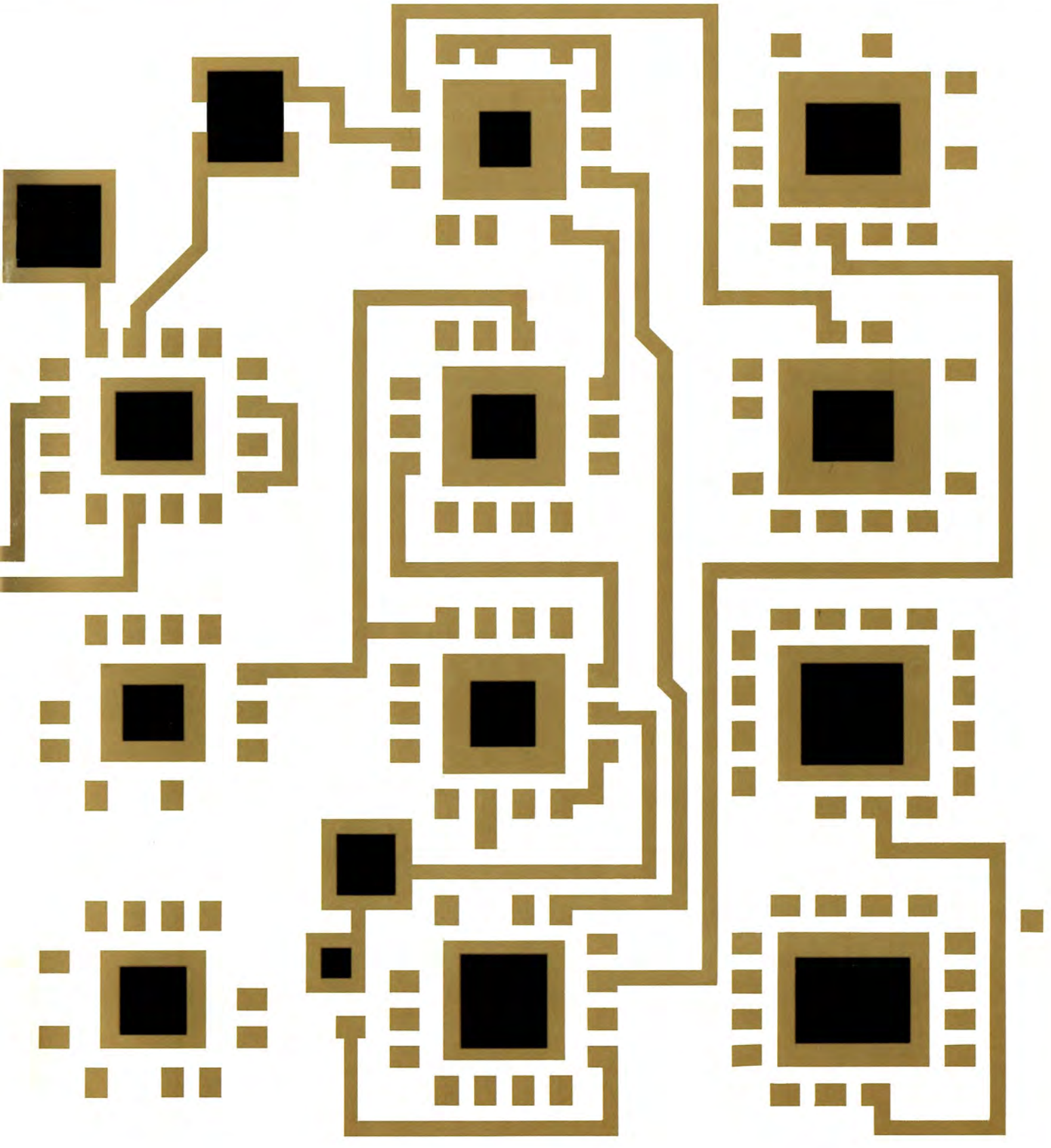
TEKTRONIX HYBRID CIRCUITS ENGINEERING



APPLICATIONS GUIDE

WHY HYBRID CIRCUITS ?

Hybrids can be considered as a very sophisticated packaging technology. In many situations, they are cost-effective alternatives to etched circuit boards. A single hybrid functional module may combine the latest components available from the semiconductor industry (including LSI bipolar and MOS IC's) with high-stability resistors, miniature capacitors, and inductors. Even laser and light-emitting diodes and phototransistors may be included. Because hybrids can be functionally tested, and resistors adjusted so that modules meet functional requirements such as minimal offset voltage, further cost savings can be effected as compared to discrete board designs requiring manual adjustments.

The reduced size and weight of hybrids are important in miniaturized equipment such as probes, and will become more significant in all portable and bench equipment in the future. As more features must be packed into existing volumes, medium-density hybrids may be the most cost-effective solution to the packaging problem.

Other advantages of hybrids include high reliability, great design flexibility, and short development times. A potentially important, but intangible, advantage of using hybrids in Tektronix equipment is that a proprietary circuit is less obvious to a competitor when it is sealed inside a package.

The next few pages describe some features of the various hybrid circuits developed in Hybrid Circuits Engineering (HCE) so that you can decide for yourself how best to use them.

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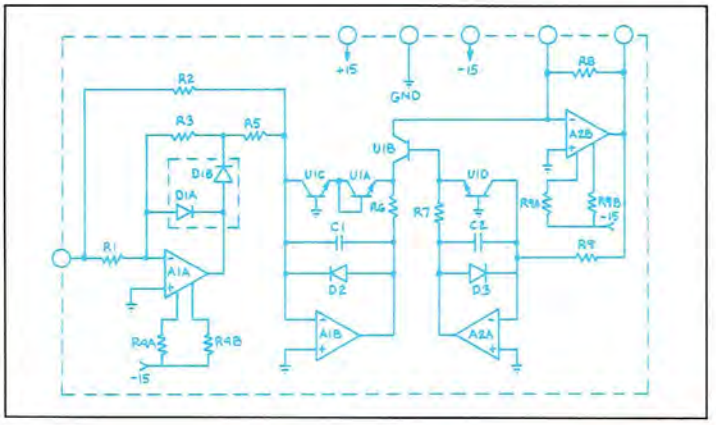


INITIATING A HYBRID CIRCUIT DESIGN

The first step in hybridizing a particular design is to optimize circuit partitioning. Factors to be considered include component density, the appropriate hybrid technology, ease of testing, power density, and thermal considerations. An important consideration in partitioning is to reduce the number of pins used on the hybrid. Dividing the circuit into functional blocks usually minimizes pin count and also optimizes the test methods used.

CHOOSING A TECHNOLOGY

The major decision is the selection of the appropriate technology. Hybrid technologies range from thick-film solder reflow, through thick-film and thin-film chip-and-wire circuits, to a high-density multichip multilayer substrate. In some cases the decision is obvious; in others, it is influenced by the choice of packages available, the cost of the manufactured hybrid, the speed with which the hybrid can be put into production, or the annual volume requirements.

The operating frequency range often determines which technology is used. Although low-value capacitors and inductors can be used in both thick- and thin-film circuitry (both as integral components and as add-on components), the upper operating frequency of thick-film resistors is generally accepted to be about 500 MHz. In addition, the use of microstrip techniques in wideband circuits is best implemented with thin-film materials.

For most circuits operating below 500 MHz, a thick-film hybrid technology is the most cost-effective approach. The solder-reflow method of attaching components to thick-film substrates is very attractive for low- to medium-complexity circuits configured in single- or dual-in-line styles. These designs have the fastest development cycle, the lowest development costs, and the lowest manufactured cost of any hybrid type. The limitation, besides the relatively low complexity attainable, is that add-on components are limited to commercially available soldered-on transistors (SOT's) and IC's (SOIC's), although regular 8-, 14-, and 16-lead dual-in-line packages can sometimes be used.

In a more sophisticated form of thick-film hybrid, silicon chips are epoxied to the substrate and wire-bonded into the circuit. Virtually all packaged devices are available in chip form, including all types of logic, microprocessor, and memory devices, precision and high-speed linear circuits, and monolithic A-to-D and D-to-A converters.

The highest density can be achieved with thick-film chip-and-wire circuitry on a multilayer substrate. Typically, four thick-film conductor layers are formed on the substrate surface to provide an interconnect and power-distribution system. Small- and medium-scale logic IC's are then bonded onto the top layer, along with chip capacitors and resistors, to produce a logic array with a density as high as 25 devices per square inch. The substrate may be packaged in a variety of ways, depending on the application. This technology specifically addresses the trend towards digital techniques throughout Tektronix instruments, and is ideally suited to CMOS and low-power Schottky TTL circuit implementation.

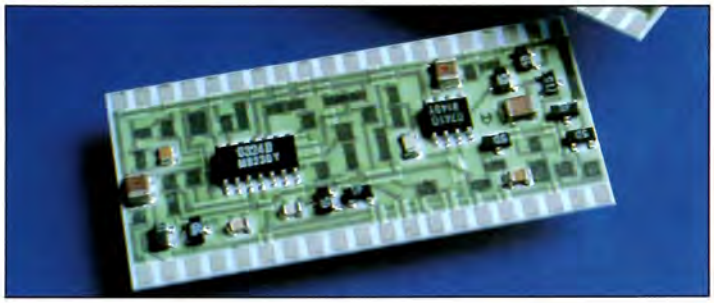
For the many applications that don't fall neatly into these categories, the collective talents of the HCE hybrid team are available to solve the problem. Many "non-hybrid" problems have also found solutions in the hybrid group: for example, the platinum-resistor temperature probe, or a connector system that is "transparent" to signals up to 5 GHz, or a concept for a 40-watt power package that uses no solder and no screws.

WHEN TO INVOLVE THE HYBRID TEAM

If you're thinking of using a hybrid in a new instrument, contact a member of the hybrid team as early as possible in your development schedule (the sooner, the better). We'll consult with your designers to establish the critical partitioning, and provide some engineering samples to you for early evaluation. Following successful testing, we'll supervise the transfer to manufacturing, and fully document and characterize your hybrid

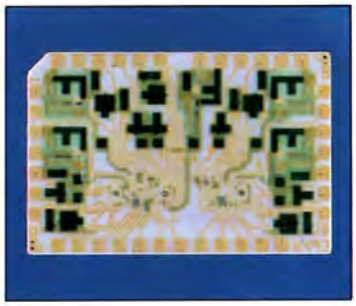
TYPICAL APPLICATIONS

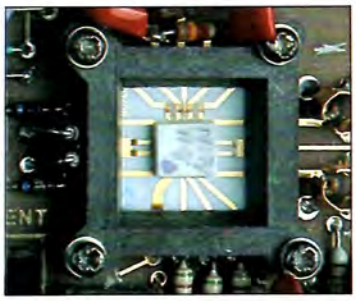
Oscilloscope Vertical Preamplifier: This thick-film dual-in-line hybrid uses SOT-23 transistors, and features low cost, low power dissipation, excellent speed, and clean response due to reduced circuit parasitic capacitances. Through-substrate capacitors are used for peaking and compensation to provide a 300-MHz system bandwidth.

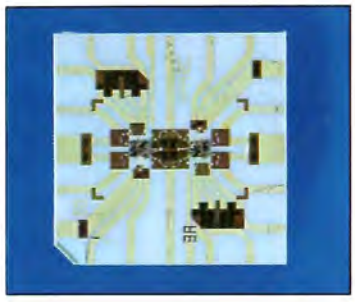


7000-Series Voltage Regulator: This very complex solder-reflow thick-film hybrid consists of two substrates placed back-to-back. Component count includes two 14-lead SOIC's, one 8-lead SOIC, 27 SOT-23 devices, 16 chip capacitors, and 60 thick-film resistors. The hybrid contains five regulators (±50V, ±15V, and +5V), all referenced to an outboard zener diode. Performance exceeds that required by 7000-series plug-ins when used with outboard bypass transistors. Each regulator is functionally trimmed to ±0.2% with respect to the reference regulator (+50V).

P.6451 Hybrid: This 5-channel data-acquisition circuit features high speed, high input impedance, variable thresholds, and a differential ECL output. Functional trimming is used to set the FET drain currents and output offset voltages; in addition, thick-film capacitors are trimmed to provide an optimally flat pulse response. The sequence of pre-testing, functional trimming, and final testing all five channels requires a total time of only 11 seconds.



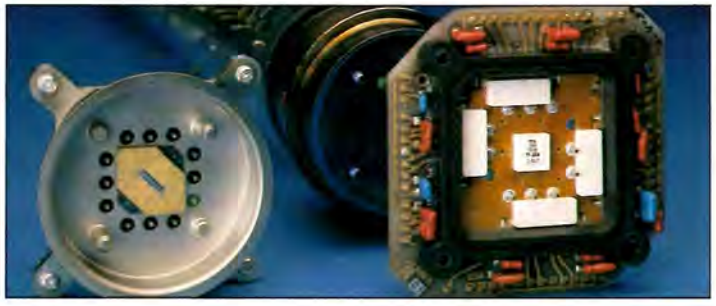




7104 Hybrids: In this 1-GHz oscilloscope, significant advances were made in the amplifiers and their interconnect system. The thin-film amplifiers use alumina and beryllia substrates, with Tektronix custom IC's and other discrete chips as active elements, to achieve the required performance. The hybrids are interconnected to the EC board by a patented connector (Hypcon) which minimizes disturbance to the microstrip lines that carry the signals.

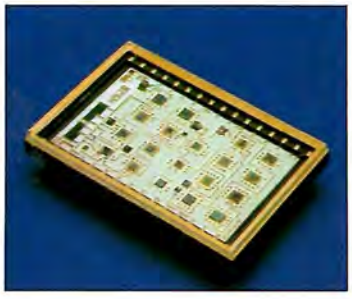
Temperature Probe: HCE designed the platinum-resistor temperature probe to be a high-accuracy, wide-range instrument. The sensor is a thin-film resistor, laser-trimmed to value, with a well-defined and reproducible temperature coefficient. The probe package is designed to provide low thermal resistance and minimal thermal mass.

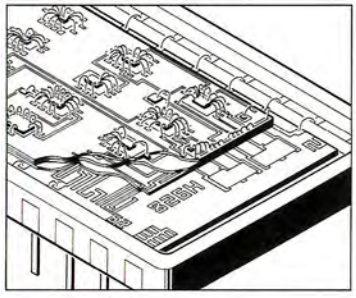
Programmable Attenuator: This component has three attenuation steps and four operating modes, selected by four Mag-Latch relays mounted on the thick film substrate. The layout was developed with the aid of two CAD programs to assist in high-frequency modeling of attenuator performance. Input impedance is 1 megohm in parallel with 15 picofarads; this time constant is trimmed to an accuracy of ±1%.



7612D Digitizer and Comparator: A unique packaging arrangement enables two hybrid devices to be placed either side of the end-cap of a cathode-ray tube, reducing the length of critical interconnecting leads, and so gives this instrument its 200MHz 8-bit digitizing capability. The digitizer hybrid contains a digitally-coded monolithic diode array, and is placed on the inside of the end-cap, where it is activated by the electron beam. The comparator hybrid consists of Tektronix comparator chips and Schottky diodes on a thin-film substrate, which slides over the end-cap pins. A Hypcon connector provides 64 lead-less connections to a printed-circuit board.

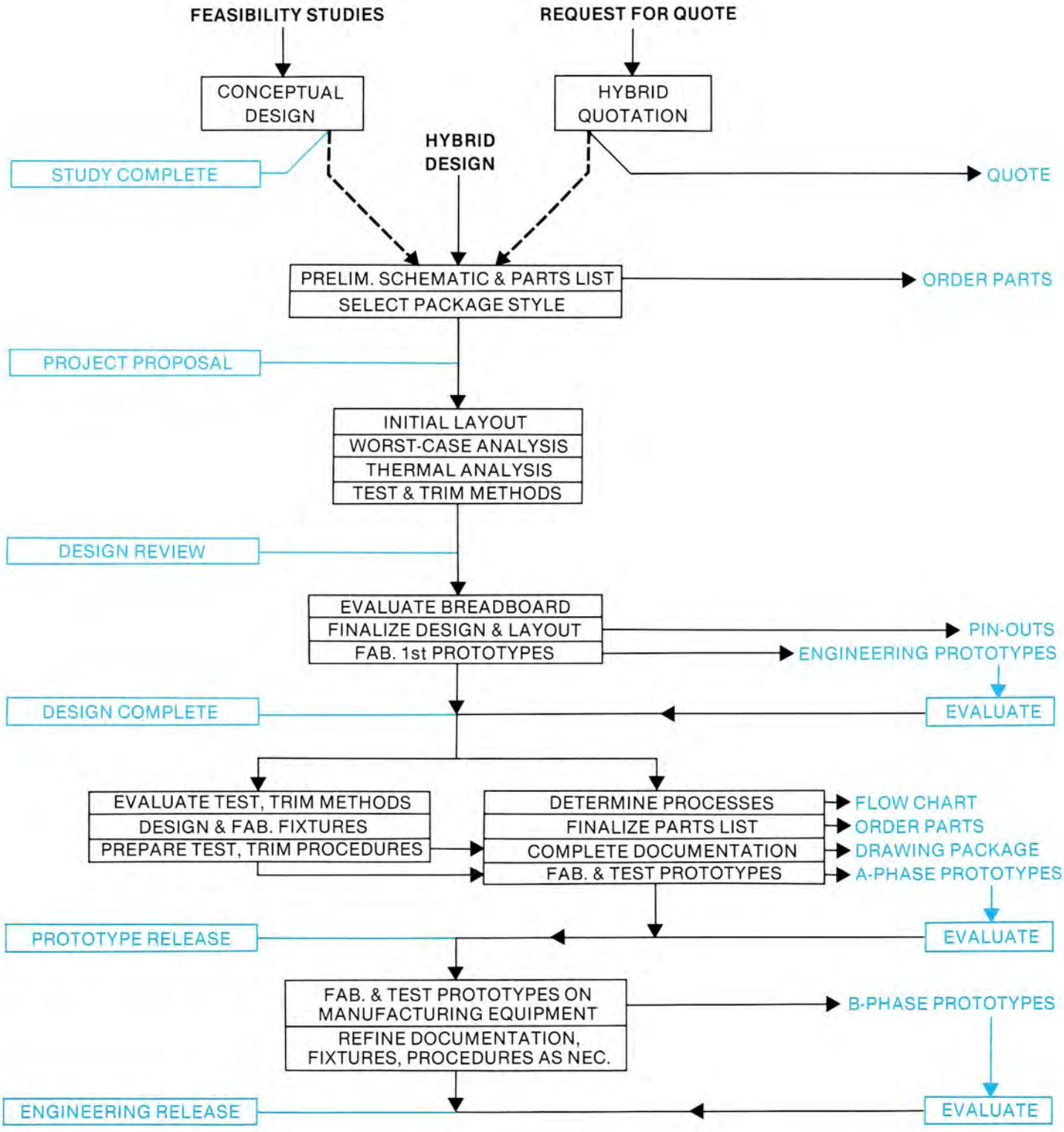
7854 Digitizer Logic: A multichip multilayer hybrid measuring about 1-3/4 × 1-1/8 inches replaces 20 square inches of EC board space. The thick-film substrate contains four gold conductor layers that form an extremely dense interconnect pattern. The top layer has pads for chip placement and interconnecting wire bonds. Nineteen low-power Schottky TTL IC's are bonded to the substrate, along with thin-film chip resistors and capacitors, and ceramic chip capacitors. The devices are interconnected to the substrate by 276 wire bonds. Four thick-film resistors, which are part of an oscillator circuit, are functionally trimmed to set the clock frequency to 10 MHz ± 0.5%.





THE DESIGN CYCLE

This flow chart represents the design cycle for a typical hybrid that utilizes standard materials and processes. Variations may be made to accommodate non-standard materials and processes.



CHARACTERISTICS OF HYBRID MATERIALS

Hybrid circuits employing thick- or thin-film substrates can accommodate an extremely wide variety of internal circuit component types and values. The charts on this page cover components constructed solely of thick- or thin-film materials. "Add-on" components compatible with hybrid assembly techniques are covered on the following page.

THICK FILM

Substrates: Material	96% Alumina (Al_2O_3) preferred 99.5% Beryllia (BeO) available
Thickness	25 ± 2.5 mils (0.635 mm), and 40 ± 4 mils (1.02 mm) preferred
Size	Up to 3" × 3" (76.2 × 76.2 mm)
Thermal conductivity, Al_2O_3	0.73 W/in-°C (0.29 W/cm-°C)
(at 100°C) BeO	4.50 W/in-°C (1.80 W/cm-°C)
Dielectric constant (1 MHz)	9.0-9.5 (Al_2O_3), 6.7 (BeO)
Dissipation factor (1 MHz)	0.0004 (Al_2O_3), 0.0003 (BeO)

Conductors:

Material	Gold	Platinum-gold	Palladium-silver
Typical use	Wire bonding, Multilayer	Solder reflow	Solder reflow, Lowest cost
Sheet resistivity	3-5 mΩ/sq.	30 mΩ/sq.	30 mΩ/sq.
Minimum line width/space	10 mils (0.25 mm) preferred 7 mils (0.18 mm) available		

Resistors: Material	duPont 1400 series
Sheet resistivity	10 Ω/sq. to 1 MΩ/sq.
Tolerance, untrimmed	±20%
trimmed	±1% to ±10% preferred ±0.25% available
Ratio tolerance, trimmed	±0.15% for similar resistors
TCR	Less than ±100 ppm/°C See curve (for large area resistors)
Ratio TCR	±15 ppm/°C typical for similar resistors
Current noise	See curve
5000 hr. drift at 125°C	Less than ±0.25%
Typical power dissipation	50 W/sq. inch in free air, greater dissipation possible by use of different materials and/or heat sinks

Capacitors:

Material	duPont 9429	duPont 4153
K factor	9	35
Typical value of 100 × 100 mil (2.54 × 2.54 mm) area	15 pf	60 pf
Tolerance, untrimmed	±20%	±20%

Inductors:

Typical value of printed spiral inductor, using 10 mil (0.25 mm) lines and spaces:

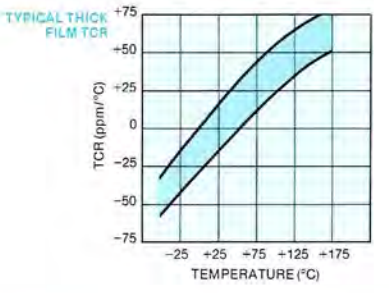
Outside diameter of 100 mils (2.54 mm):	4.5 nanohenries
Outside diameter of 200 mils (5.08 mm):	40.0 nanohenries

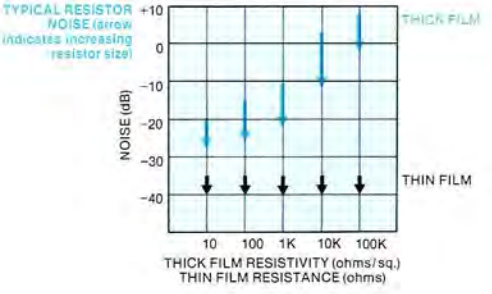
THIN FILM

Substrates: Material	99.6% Alumina (Al_2O_3) preferred 7509 glass and fused silica available
Thickness	25 ± 2 mils (0.635 mm) preferred 40 ± 4 mils (1.02 mm) available
Size	Up to 3" × 3" (76.2 × 76.2 mm)
Thermal conductivity (Al_2O_3)	0.73 W/in-°C (0.29 W/cm-°C)
Dielectric constant (1 MHz)	9.7-10.1 (Al_2O_3), 5.8 (glass), 3.8 (fused silica)
Dissipation factor (1 MHz)	0.0001 (Al_2O_3), 0.001 (glass), 0.0002 (fused silica)

Conductors: Material	Gold
Sheet resistivity	5 mΩ/sq.
Minimum line width/space	25 micron (1 mil) preferred, 6 micron (.25 mil) available

Resistors: Material	Nichrome
Sheet resistivity	10, 25, 50 Ω/sq.
TCR	+150 ppm/°C max, +85 ppm/°C typical
Ratio TCR	±5 ppm/°C max
Minimum line width	25 micron (1 mil) preferred, 6 micron (.25 mil) available
Tolerance (untrimmed)	±12%
(trimmed)	±0.1% (analog trim), ±0.005% (digital trim)
(ratio, trimmed)	±0.005%
Maximum operating temperature	+150°C
5000 hr. drift at 125°C	Less than 0.1%
Current noise	Less than −30 dB





COMPATIBLE COMPONENTS

A wide variety of "add-on" components can be used in hybrid circuits to supplement the conductor-resistor-capacitor network that is integral with the substrate. Virtually all semiconductor components are available from most manufacturers as passivated chips for use in "chip-and-wire" hybrids, from the simplest diodes and zeners to linear IC's, all forms of logic IC's, and microprocessor and memory chips.

A key consideration in the conversion to a hybrid design is to determine what parameters the manufacturer will be able to measure (that is, probe) in chip form. All standard chips are available at reasonable cost when purchased "dc wafer probed" to their data-sheet specifications (however, there are limits on probe capabilities, such as minimum current of 100 nA and current gains up to 500 mA). Special probe requirements, such as ac testing or parameter matching, add significantly to the cost and lead time of the chips.

Other components that are available include thin-film chip resistors, resistor networks, capacitors and R-C networks, ceramic chip capacitors, and chip inductors. Although tantalum chip capacitors are available, it is usually economically advantageous to locate components such as tantalum capacitors and large inductors outside the hybrid.

Special devices known as SOT (Soldered-on transistor) and SOIC (Soldered-on IC) are available for use in solder-reflow hybrids, but the range of these devices is not as extensive as for chips. One of the limitations of the solder-reflow technology is that chips can't be used unless they are first packaged into a ceramic chip carrier. Although this extra step adds considerable expense, it enables the chip to be pre-tested and even burned in, and can therefore be a useful technique for complex LSI and memory chips.

The tables on this page indicate preferred component types, many of which are available as Tektronix part numbered devices.

HINTS FOR A SUCCESSFUL HYBRID DESIGN

- Start out with a clear conception of what function is required, and provide a tentative performance specification.
- Bring in the hybrid design team as soon as practical in a new program, to lead to optimum partitioning, component selection, etc.
- Partition complex circuits into functional blocks to facilitate testing, and bring out test points or assign probe points wherever advantageous to aid in trouble-shooting.
- Avoid large capacitors and inductors, and resistor values covering more than three decades of resistance.
- Use resistor ratios rather than absolute values in critical parts of a circuit.
- Select from lists of preferred components where possible; lead times of new components can become the pacing item of a program.
- Use a standard package configuration where possible.
- Leave definition of pin-outs to the hybrid designer to allow maximum flexibility in the layout.

TABLE 1
SEMICONDUCTOR DICE

Virtually any semiconductor discrete device is available in chip form, including diodes (except some very-low-current devices), zeners, Schottky diodes, transistors, and FET's.

Linear IC chips are available from most popular IC manufacturers, as are CMOS, TTL, LSTTL, ECL and other logic families, including LSI devices.

TABLE 2
THIN-FILM CHIP RESISTORS

Available as standard chips, tantalum nitride on silicon, 30 mils (0.76 mm) square in the range 4.7 ohms to 1 megohm, or 40 mils (1.02 mm) square from 1 megohm to 24 megohms. Also available as custom chips of resistor arrays, utilizing tantalum nitride (zero to −150 ppm/°C) or nichrome (±50 ppm/°C) films on silicon. Typical TCR tracking is ±2 ppm/°C for such arrays.

THIN-FILM CHIP CAPACITORS

Available as standard chips in three sizes: 20 mils (0.51 mm) square (4.7 pF to 51 pF), 40 mils (1.02 mm) square (56 pF to 430 pF), and 55 mils (1.40 mm) square (470 pF to 1000 pF). Working voltage varies from 25 to 200 depending upon capacitance value. TCC is 45 ± 20 ppm/°C. Also available as custom chips of capacitor arrays, or resistor-capacitor arrays.

CERAMIC CHIP CAPACITORS

Standard devices are available in a wide variety of sizes; some preferred types include:

NPO (TCC less than ±30 ppm/°C)
90 × 60 mils (2.29 × 1.52 mm), 1.0 pF to 680 pF, 50 V

BX (temperature change ± 15%)
90 × 60 mils (2.29 × 1.52 mm), 120 pF to 0.015 μF, 50 V
135 × 105 mils (3.43 × 2.67 mm), 0.047 μF to 0.1 μF, 50 V

Many other size and value combinations are also available, as are capacitor chips specially designed for vhf and microwave applications.

TABLE 3
SOT

These devices, designed for solder-reflow applications, are available in two styles, covering a wide range of types:

SOT-23 (300-mW dissipation)
- general-purpose diodes, including 1N914 in single and dual configurations
- a family of zener diodes corresponding to 1N5226B series
- most popular transistor types, including 2N918, 2N2222A, 2N2369, 2N2907A, 2N3904, 2N3906, 2N4416, 2N4957

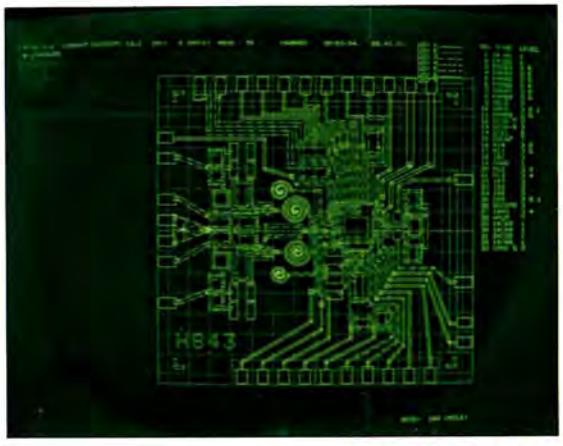
SOT-89 (1W dissipation)
- BFQ17 (npn, f_T = 1.2 GHz)

SOIC

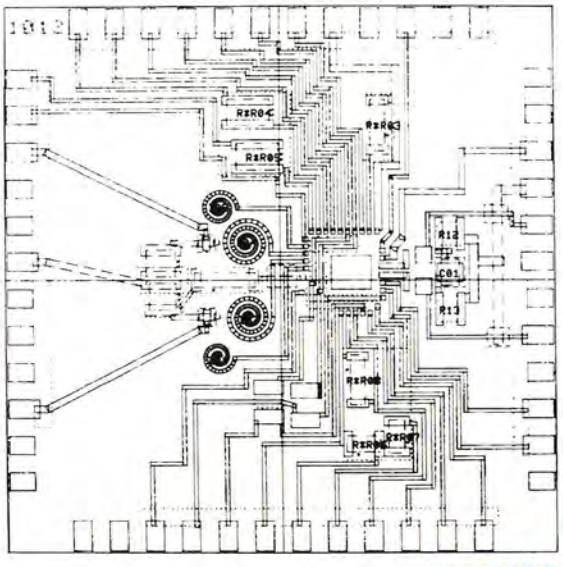
A number of general-purpose linear IC's are available, including:

- op-amps: 741 (single, dual, and quad), 308, NE530, NE5534
- comparators: 311, 319, 339
- regulators: 723
- specials: 555 (timer), 1408 (multiplying DAC), 1488/9 (line driver/receiver)

COMPUTER-AIDED LAYOUT



TERMINAL DISPLAY



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A software package known as HCAD has been developed as a design aid for custom hybrid circuits. The software resides on the Cyber 175 computer, and is used by engineers throughout the company via local terminals. This approach is an effective way to disseminate rules and to standardize designs, which is especially important when a large variety of design requirements and many different process alternatives are available.

The system automatically designs hybrid components (resistors, capacitors, and inductors) from schematic inputs. These components are designed from stored models that take into account laser trimming, power dissipation, voltage gradient, minimum sizes, materials interaction, layer misalignment, process variation, and any other applicable design rules. When necessary, the user can interactively redesign the components as the layout progresses. A component library is also available for special components or for non-hybrid applications.

When the components have been designed, they are interactively located and interconnected manually on the CRT screen with interactive graphics. Typical commands are translate, rotate, duplicate, mirror image, add, and kill. When the design is complete, the system writes a magnetic tape that can be run directly on a pattern generator to create artwork.

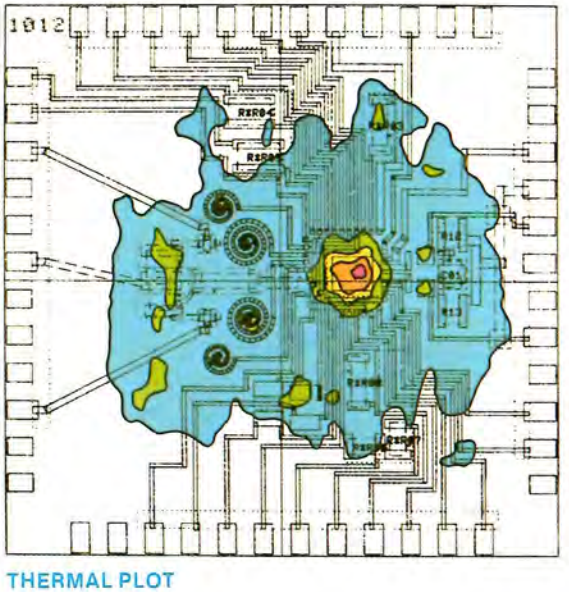
HCAD can also be used to analyze the design. Geometry data is extracted and used in other analysis programs. These programs allow for three-dimensional, steady-state temperature predictions, potential-field analysis for resistor and laser trimming design, and nodal capacitance-to-ground calculations.

The software also aids the documentation of each design. A labeled plot of the layout can be provided with title blocks, color selection, and process specifications. This documentation is used for check plots as well as for final process drawings.

THERMAL MANAGEMENT

One part of the HCAD system consists of a thermal analysis program which allows temperature predictions to be made for many typical hybrid designs and package styles.

For hybrids that require more extensive thermal considerations, the HCE Thermal Lab can provide other analysis programs, together with many different measurement techniques. These techniques include pulse sensing of transistor junctions, microminiature thermocouples, and infrared scans which provide an isothermal map of the entire surface of a hybrid, with a maximum temperature resolution of 0.1°C and a spot size variable down to 1.2 mils.

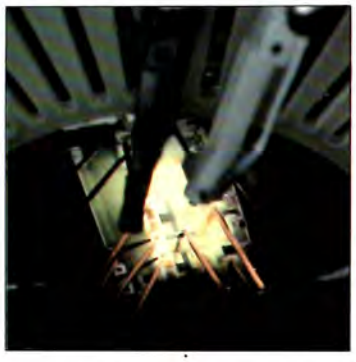


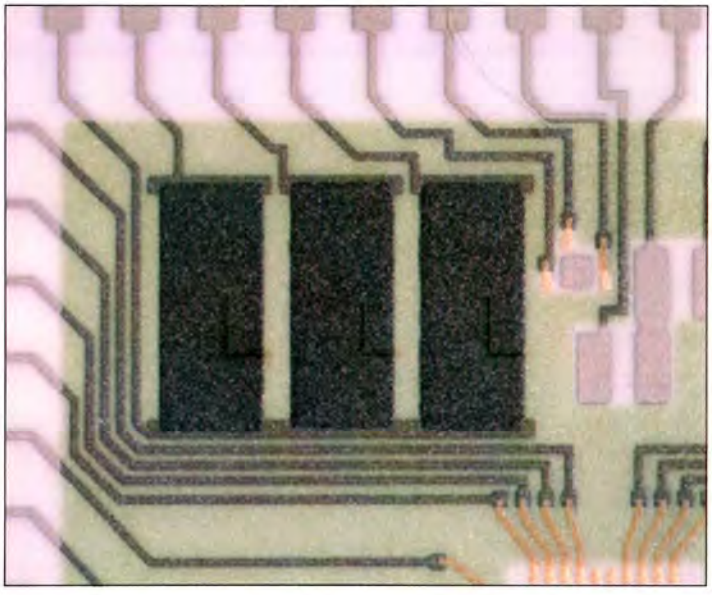
THERMAL PLOT

AUTOMATED TEST AND TRIM

Besides developing special test instrumentation and software for hybrid products, HCE can also perform many related functions such as circuit characterization, trim sensitivity analysis, and design of special mechanical test fixturing.

The primary trimming equipment used is the ESI model 44 laser trimming system which consists of a computer-controlled laser plus positioning and measurement systems. It is capable of 2.5-micron (0.1-mil) resolution over a 3-inch (76.2-mm) square area, cutting a kerf variable from 5 to 100 microns (0.2 to 4 mils).





Trimming resistors to value on a substrate before other components have been added is called passive trimming. Both resistors and capacitors can be adjusted by this method, either to absolute values or to ratio requirements. Trims are accomplished in from 0.2 to 5 seconds per trim.

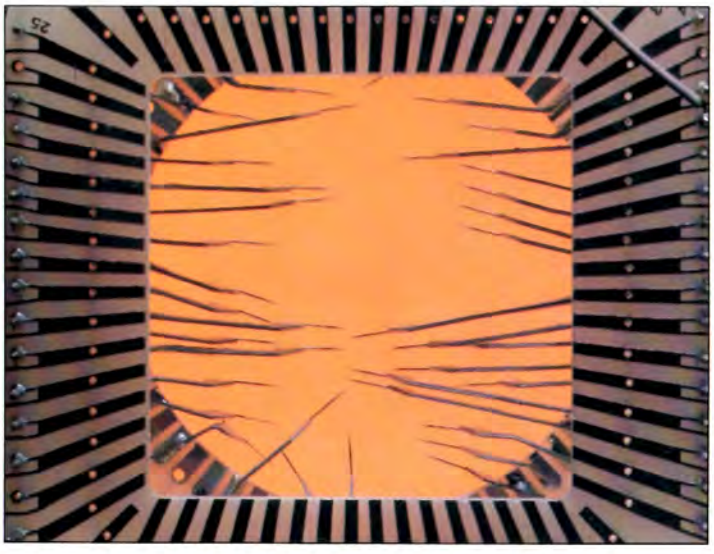
Resistors and capacitors can also be adjusted to provide a specific circuit parameter value. This functional trimming is also called active trimming because the adjustment is made with the circuit under power, or "active". This can be a very powerful technique, since it allows a hybrid circuit to be pre-adjusted to a particular specification, and might remove the requirement for a manually adjusted potentiometer in the final test sequence.

Typical circuits that benefit from functional trimming include amplifiers, attenuators, and analog-to-digital and digital-to-analog converters. Common parameters adjusted include gain, offset, impedence, and transient response. Trim times are from 1 to 5 seconds per trim.

Another function within HCE is test development, which provides circuit characterization and testability verification on hybrid products. Typically, this function is carried out on a general-purpose automatic test system.

Test measurement capability matches that of the laser-trim measurement capability. However, the availability of more advanced handling equipment for the test systems often provides significantly enhanced throughput rates at the test station.

In addition, HCE can develop custom system instrumentation for unusual circuit functions, such as high-frequency input-impedance measurements.

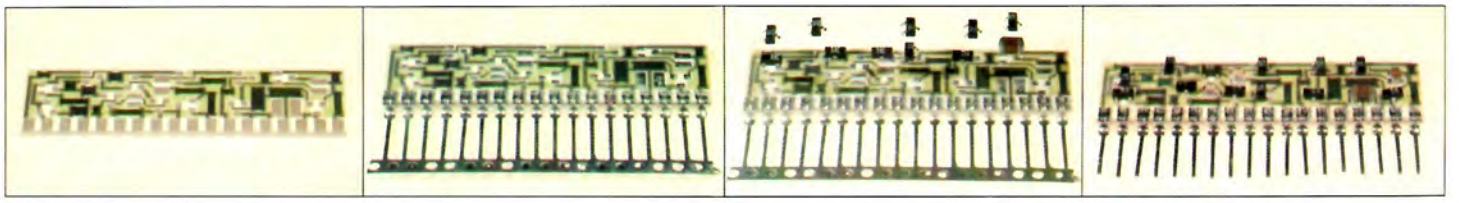


The test-and-trim automatic systems can provide an extremely wide range of circuit stimuli, such as precision dc voltages and currents, wideband ac signal sources, high-speed pulse sources, and digital imputs. Measurement capabilities include very accurate dc voltages, currents, and resistance, and moderate-accuracy ac measurements, capacitance, and inductance. Transient and high-frequency phenomena can be measured with a sampling waveform digitizer, and a network analyzer is available for rf measurements.

HYBRID ASSEMBLY

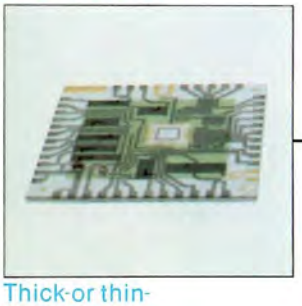
Hybrid Circuits Engineering has complete prototyping facilities in all forms of hybrid assembly, including solder reflow, chip-and-wire assembly, and hermetic and non-hermetic sealing. The following flow charts indicate the most popular assembly techniques.

SOLDER REFLOW

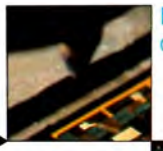


Thick-film substrate | Attach components | Solder reflow | Attach lead frame

CHIP-AND-WIRE

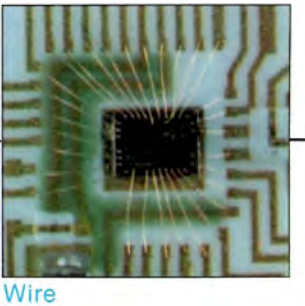


Thick-or thin-film substrate

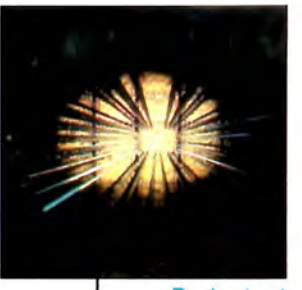


Eutectic die mount

Epoxy mount die and all passive components

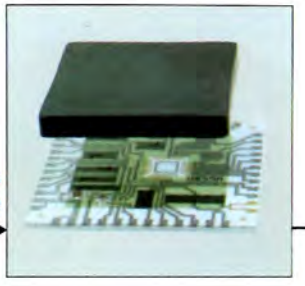


Wire bond

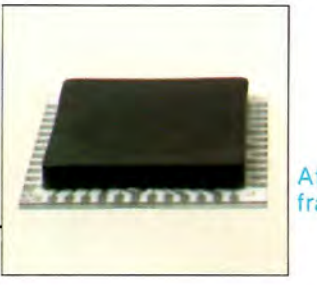


Probe test and functional trim (optional)

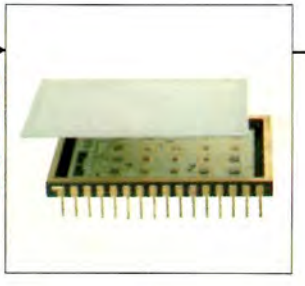
NON-HERMETIC



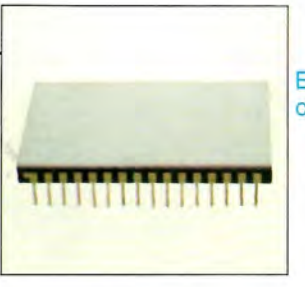
Epoxy ceramic cover to substrate



Attach lead frame (optional)



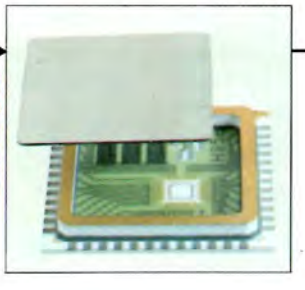
Epoxy substrate into ceramic package, wirebond to internal leads



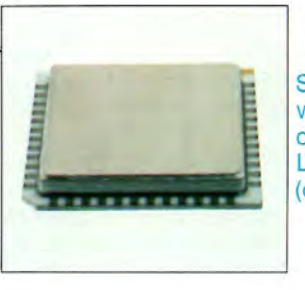
Epoxy cover

HERMETIC

May use ceramic package as above, but with metal ring frame, and with cover soldered or welded to frame

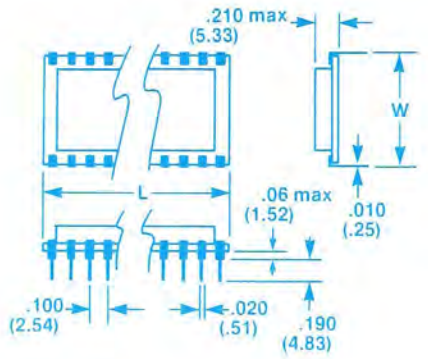


Glass-sealed ceramic wall frame (must be assembled prior to component attach)



Soldered or welded cover. Lead frame (optional)

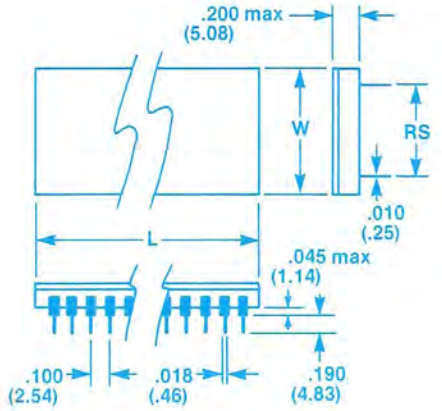
PREFERRED PACKAGE STYLES



LEADS	STYLE	L	W
10	SIP	1.00 (25.40)	0.50 (12.70)
15	SIP	1.50 (38.10)	0.50 (12.70)
24	DIP	1.20 (30.48)	0.60 (15.24)
26	DIP	1.50 (38.10)	0.75 (19.05)
32	DIP	1.80 (45.72)	0.90 (22.86)
48	QUIP	1.50 (38.10)	1.50 (38.10)
64	QUIP	1.75 (44.45)	1.85 (46.99)

- Drawing shows DIP configuration
- Single-in-line, dual-in-line & quad-in-line available in many other sizes
- Thick film non-hermetic only, chip & wire or solder reflow
- Dimensions in inches (mm)

This package is also available without lead frames for use in microminiature edge connectors for single-in-line hybrids, or "chip-carrier" sockets for hybrids with pads on all four sides (up to 64 pads available).

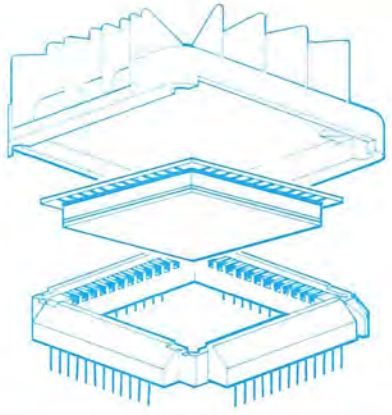


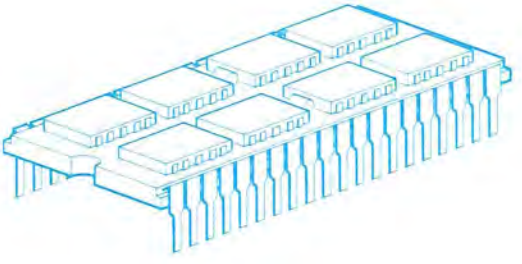
LEADS	L max	W max	ROW SPACING
16	0.925 (23.50)	0.520 (12.22)	0.300 (7.62)
18	1.025 (26.04)	0.520 (12.22)	0.300 (7.62)
24	1.325 (33.66)	0.820 (20.83)	0.600 (15.24)
32	1.730 (43.94)	1.120 (28.45)	0.900 (22.86)
40	2.135 (54.23)	1.120 (28.45)	0.900 (22.86)
62	2.345 (59.56)	1.425 (36.20)	1.1 × 2.0 * (27.94 × 50.80)

- Available as hermetic or non-hermetic
- Can use thick or thin film, chip & wire
- Dimensions in inches (mm)

* Quad-in-line — all others dual-in-line

CUSTOM PACKAGE STYLES





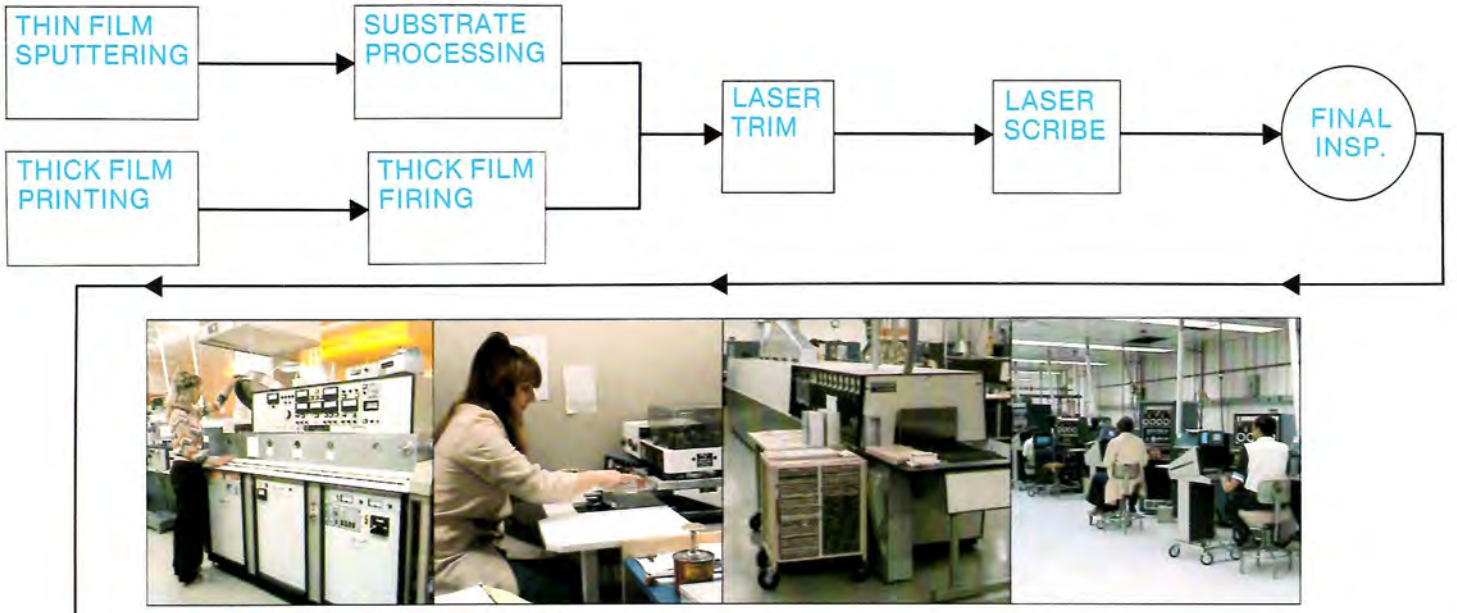
In addition to many variations on these preferred styles, HCE is capable of developing innovative solutions to your special packaging needs. In one example, when the preferred styles were not optimum, a special package was designed which combined an integral heat sink and a high-frequency interconnect system, yet still provided easy field replacement. Many unusual packages have also been developed to solve the unique problems associated with using hybrids in probes.

HCE can also look at your total system packaging requirements and generate concepts that integrate hybrid circuits into a complete subsystem. The subsystem may include, for example, connectors, a heat sink, power devices, keyboards, displays, and flexible circuitry in addition to the hybrids. The use of chip-carriers may also be considered for use in arrays of LSI devices; chip-carriers are especially suited to memory arrays.

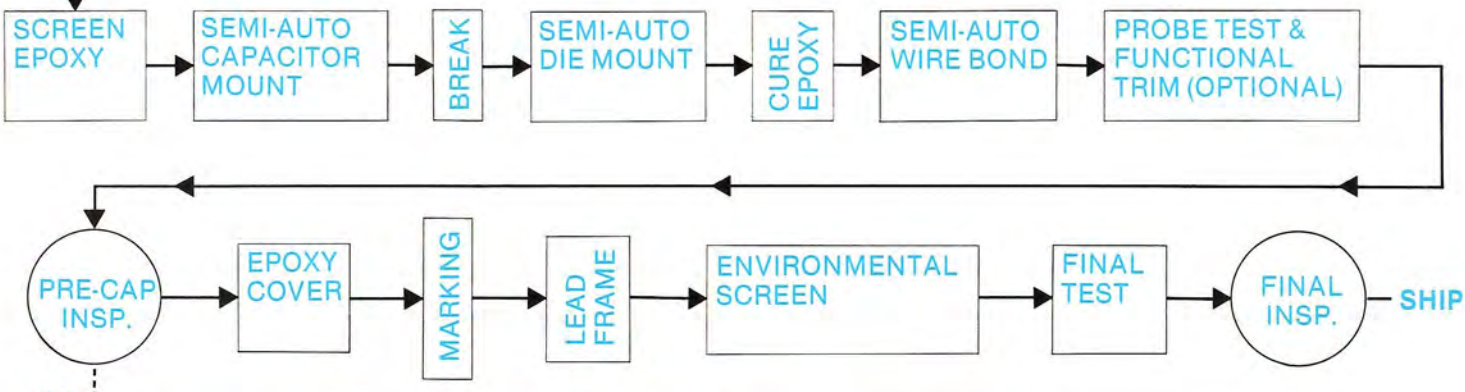
MANUFACTURING FACILITIES

After a hybrid to be used in a Tektronix product has been fully developed and documented, the design is transferred to Hybrid Circuits Manufacturing (part of the Technology Group). This well-equipped facility is sufficiently staffed to produce hybrids in high volume, with a capacity in excess of 30,000 finished units per month. It is organized into two areas...

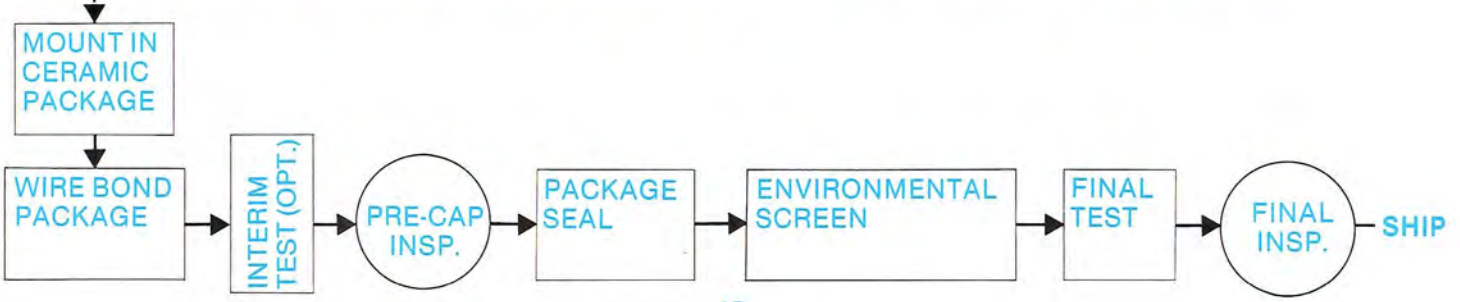
SUBSTRATE FABRICATION



ASSEMBLY AND TEST



ALTERNATE METHODS FOR FINAL ASSEMBLY



The Tektronix hybrid manufacturing organization includes an extensive quality and reliability group, whose primary functions are to establish that hybrids initially meet or exceed a certain level of reliability, and that they maintain that level throughout their production run. The various functional groups and their responsibilities are as follows:

Qualification

- Generic testing to verify reliability of new hybrids to the appropriate reliability classification.
- New process qualification by characterization and matrix testing.
- Quality conformance by monitoring current production hybrids for conformance to predetermined standards.

Quality Assurance

- Material control through Incoming Inspection.
- Product quality control by QA gates which monitor the effectiveness of in-process QC inspections.
- Process control through QA audits of equipment and processes.
- Monitoring of environmental screens (such as burn-in) applied to production hybrids when deemed necessary to assure a required level of reliability.

Failure Analysis

- Identification of failure modes and mechanisms for fault analysis.
- Available analysis techniques include:

Wet chemistry	Plasma etching
X-ray	Die shear
Micro/macro cross-sectioning	Probe stations
Particle impact noise detection	Microscopes

Analytical Services

- Electrical and material analyses.
- Microelemental analyses.
- Available services include:

  Scanning electron microscopes
  Elemental X-ray analysis

Reliability Design Guidance

- Feedback on production and new product reliability evaluation to upgrade design models and guidelines.

Reliability Screens

- Assistance to Design, QA, and Manufacturing engineers on reliability problem areas and development of adequate environmental screens to help overcome these problems.

Field Reliability Reports

- Evaluation of factory and field returns and publication of reports.

IN SUMMARY...

We hope this brief overview of hybrids at Tektronix has whet your appetite for more information. Whether your application is a very basic space-saver hybrid, or the innovative use of new materials and techniques, we would like to discuss it with you in greater depth. And, of course, you are welcome to tour HCE's facilities at any time.
Your first step is to call one of the hybrid team...soon.

FOR FURTHER INFORMATION, WRITE OR PHONE:

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P.O. Box 500
Beaverton, Oregon 97077
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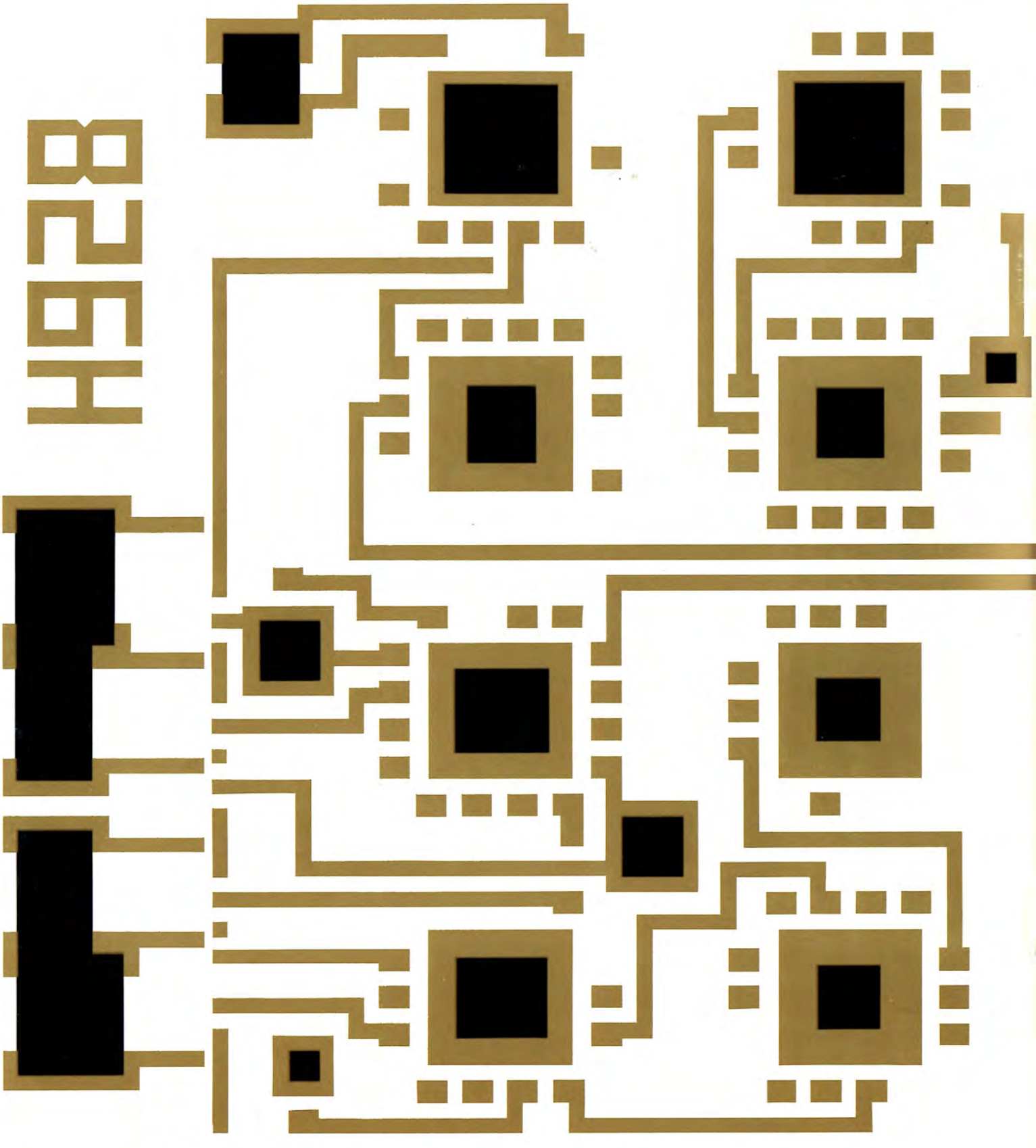

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