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PDP-7

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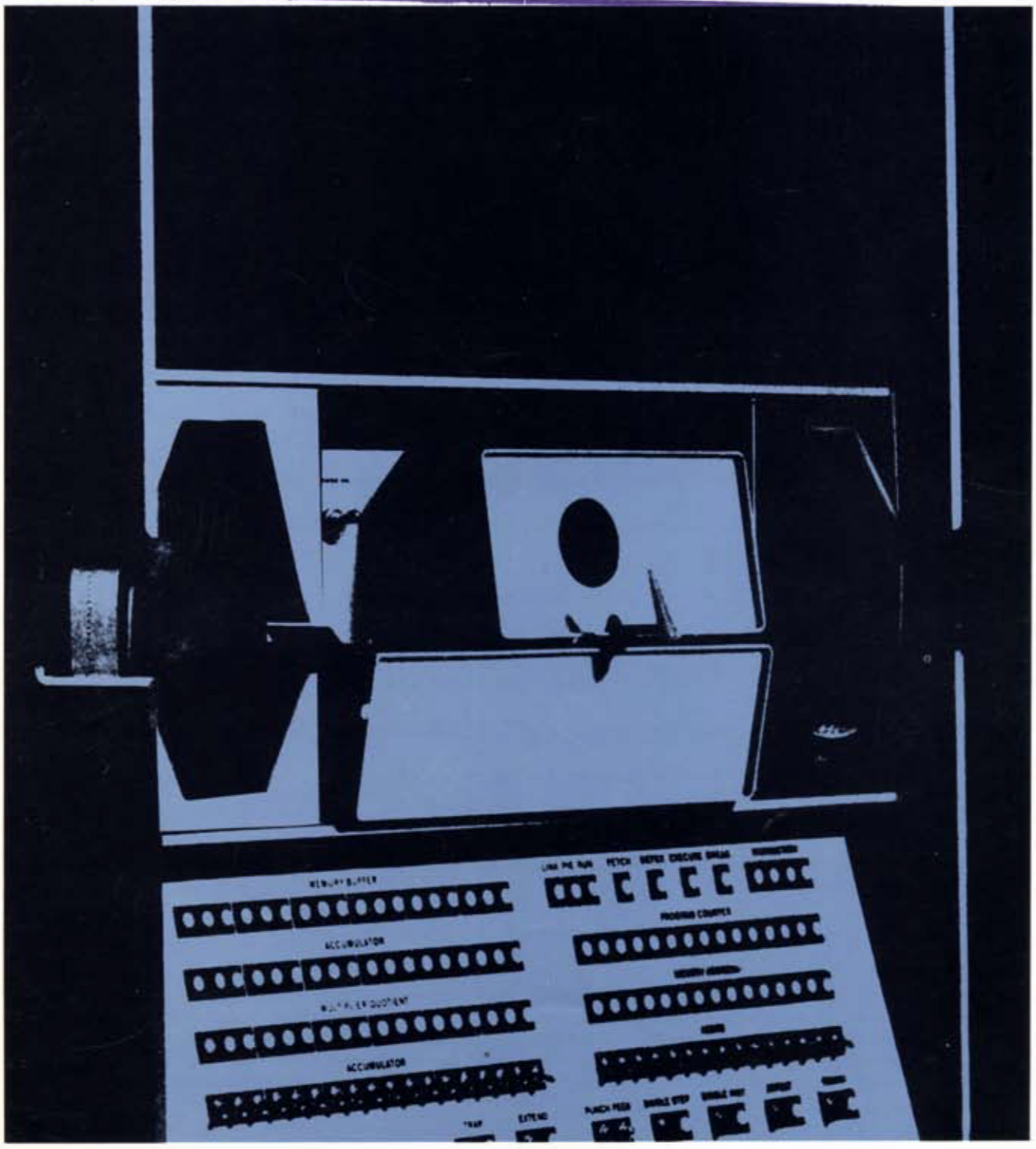


DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PROGRAMMED DATA PROCESSOR-7 (PDP-7) *is a general purpose, solid state, digital computer designed for high speed data handling in the scientific laboratory, the computing center, or the real time process control system. PDP-7 is a single address, fixed 18-bit word length, binary computer using 1's complement arithmetic, and 2's complement arithmetic to facilitate multi-precision arithmetic. A random access magnetic core memory with a complete cycle time of 1.75 microseconds is used to achieve a computation rate of 285,000 additions per second. Other features of the basic PDP-7 system include:*

SILICON FLIP CHIP MODULES are used throughout PDP-7. Cost of spares is low.

FIELD TESTED SOFTWARE includes an advanced FORTRAN compiler, a symbolic assembler, floating point arithmetic, and program compatibility with the field tested PDP-4 program library.

MODULAR DESIGN permits the addition of peripheral devices simply by plugging in modules and cables.

COMPREHENSIVE I/O CONTROL, as supplied, connects to 64 input and output devices and includes an Input/Output Control, a Program Interrupt, Data Interrupt, I/O Trap, I/O Status, I/O Skip and Real Time Clock. Easily expandable to any size.

I/O TRAP hardware supplied to permit the programming of a time-shared system.

MULTIPLE AUTO-INDEXING using eight memory locations simplifies programming and increases the speed of table look-up and other routines.

FULLY PARALLEL internal operations simplify maintenance and increase reliability.

DATA INTERRUPT at data transfer rates up to 570,000 words per second with direct access to core memory and without disturbing arithmetic registers.

PROGRAM INTERRUPT frees processor from time-dependency on external devices.

ENVIRONMENTAL TOLERANCE permits computer and peripheral equipment to operate without air conditioning on 115 $\pm$10 volts AC, 60 $\pm$0.5 cps.

ASCII STANDARD 8-bit CODE is used with Model 33KSR teleprinter.

ECONOMICAL MEMORY EXPANSION up to 32,768 words is provided for.

READ-IN SWITCH loads a block of words from binary paper tape into memory and initiates program execution.

HIGH SPEED OPERATION with a memory cycle time of 1.75 microseconds and add time of 3.5 microseconds.

PROGRAMMED TAPE CONTROL permits program control of punch power.

INDIRECT ADDRESSING simplifies subroutine linkage.

MICROPROGRAMMING saves program execution and preparation time by coding instructions capable of multiple operations.

Parallel operation and parallel data flow using integrated circuit modules assure the highest degree of computer reliability possible. All modules, sub assemblies and then the final computer are given a thorough test and check-out before being released.

Built into each PDP-7 is a network for marginal test of computer sub-sections. Two features of the marginal test system make routine checks fast and accurate: The marginal check voltage is continuously variable, and all working registers are displayed simultaneously on the console lights.

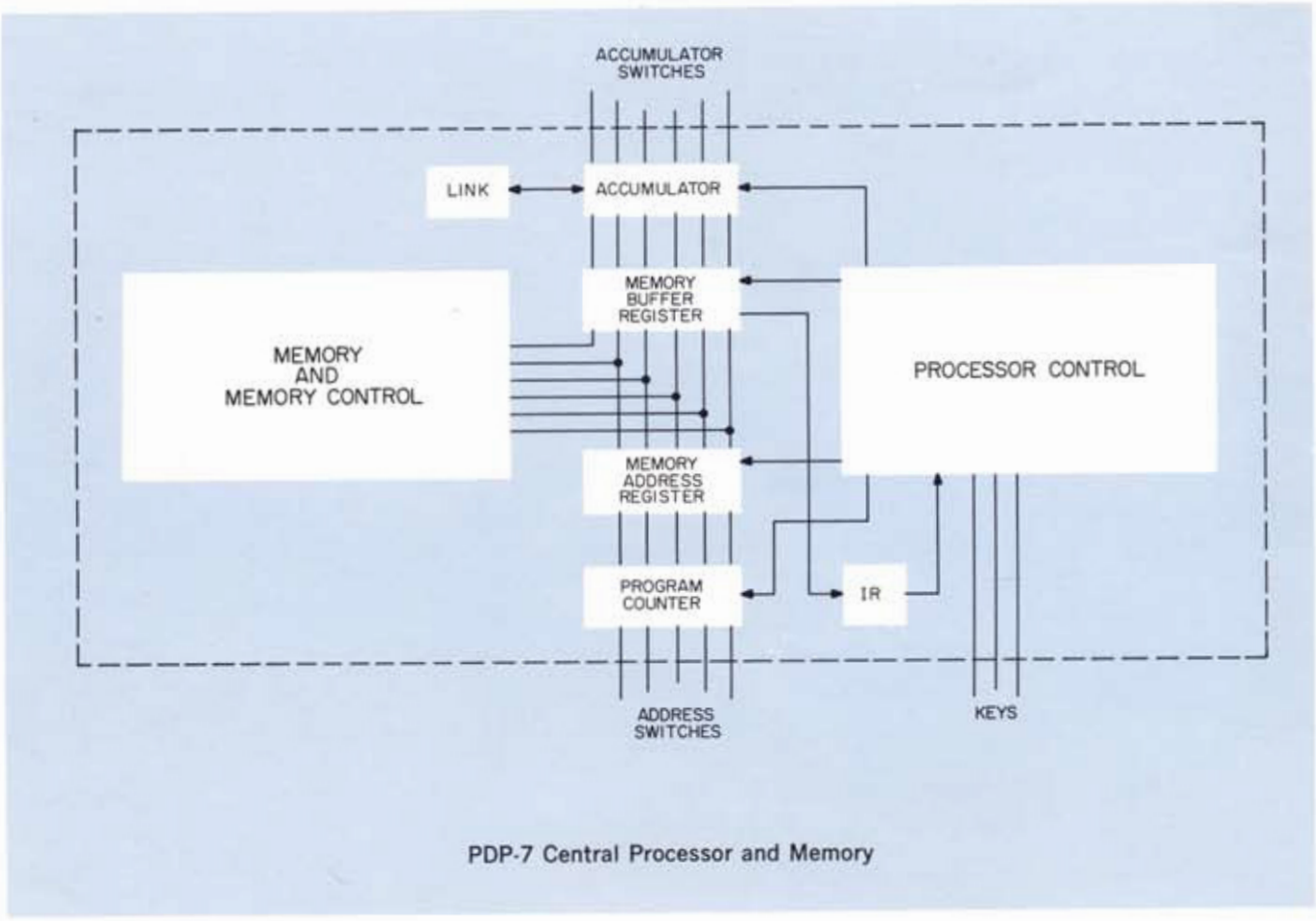
BASIC PDP-7

The basic PDP-7 is a highly effective system in a minimum configuration. The basic PDP-7 includes:

Central Processor and Control Console
4096 Word Core Memory
Input/Output Control with
- Device Selector (up to 64 I/O connections)
- Information Collector (seven 18-bit channels)
- Information Distributor (six 18-bit channels)
- Program Interrupt
- Data Interrupt
- I/O Trap
- I/O Skip Facility
- I/O Status Check
- Real Time Clock

High Speed Paper Tape Reader (300 cps)
High Speed Paper Tape Punch (63.3 cps)
KSR 33 Teleprinter (10 cps)

Programming Aids
- FORTRAN Compiler
- Symbolic Assembler
- Editor
- Debugging System
- Maintenance Routines
- Library



PDP-7 Central Processor and Memory

PROCESSOR

The processor performs logical and arithmetic functions, provides access to and from memory and controls the flow of data to and from the computer. It consists of the processor control, the memory, memory control and six other active registers (see diagram).

ACCUMULATOR (AC) is an 18-bit register which performs arithmetic and logical operations on the data and acts as a transfer register through which data passes to and from the I/O buffer registers.

LINK (L) is a 1-bit register used to extend the arithmetic facility of the accumulator.

MEMORY ADDRESS REGISTER (MA) is a 13-bit register which holds the address of the core memory cell currently being used.

MEMORY BUFFER REGISTER (MB) is an 18-bit register which acts as a buffer for all information sent to or received from memory.

INSTRUCTION REGISTER (IR) is a 4-bit register which holds the operation code of the program instruction currently being performed.

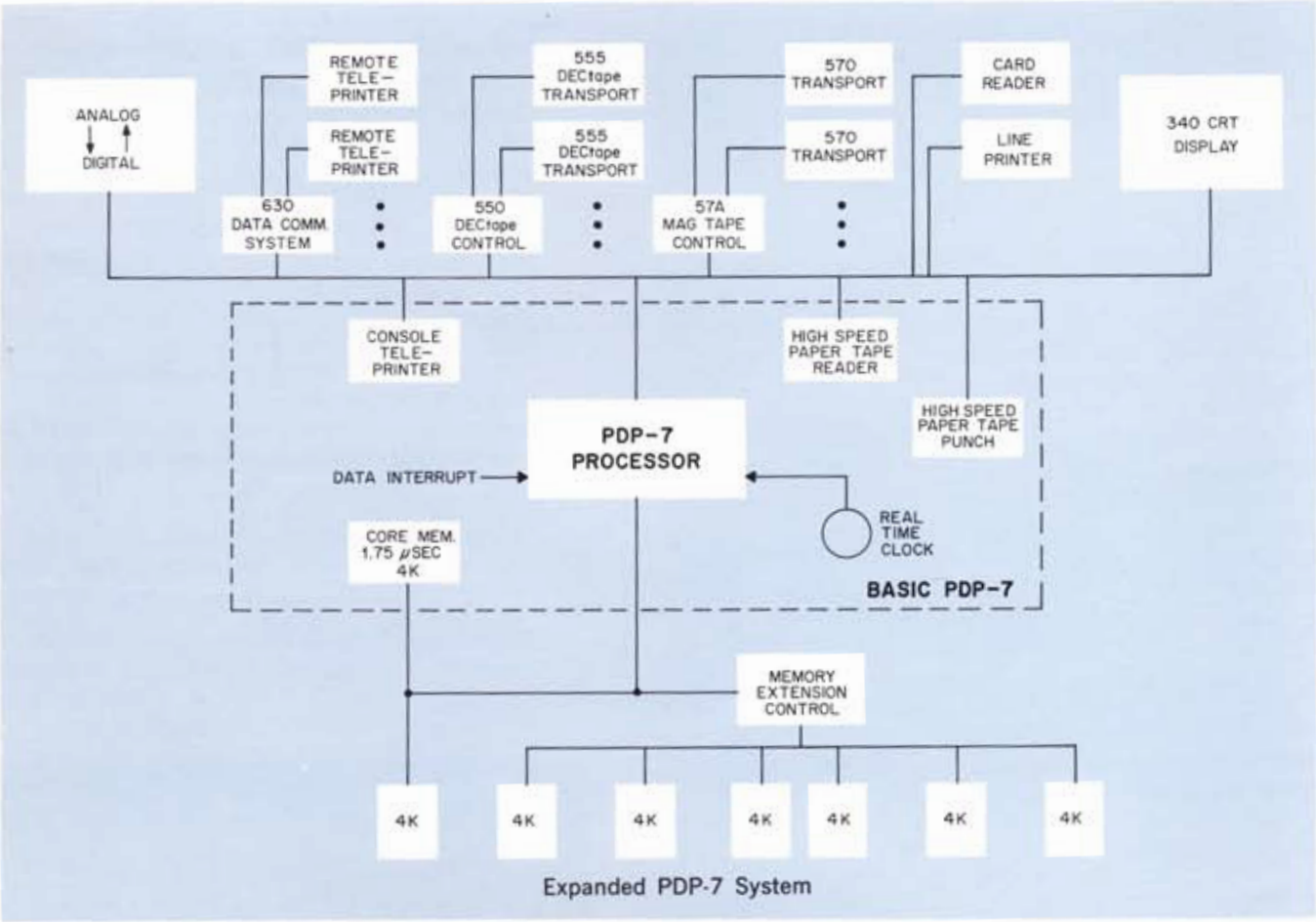
PROGRAM COUNTER (PC) is a 13-bit register which holds the address of the next memory cell from which an instruction is to be taken.

MEMORY

The high speed random access memory is a 4096 word coincident-current core module with a cycle time of 1.75 microseconds. In one cycle the memory control retrieves an 18-bit word stored in the memory cell specified by the memory address register, writes the word by a parallel transfer into the memory buffer register, and rewrites the word into the same memory cell.

INPUT/OUTPUT CONTROL

The I/O control links up to 64 input and output stations by lines to the central processor, calls the stations, and collects and distributes the input/output data. It also controls the interleaving of data during a data interrupt, senses the status of I/O devices and skips instructions based on this status, traps IOT (input-output-transfer) instructions initiating a program break, and generates real time signal pulses for use by external peripheral equipment.



Expanded PDP-7 System

PROCESSOR OPTIONS

Core Memory Module Type 147 extends the memory capacity of the PDP-7 from 4096 words to 8192 words.

Core Memory Extension Control Type 148 allows the expansion of the PDP-7 memory from 8192 to 32,768 words in increments of either 4096 or 8192 words, using the Type 149 Memory Modules. The Type 148 includes an Extended Program Counter, an Extended Memory Address Register, and an Extend Mode Control.

Extended Arithmetic Element Type 177 is a standard option for the PDP-7 which facilitates high-speed multiplication, division, shifting, and register manipulation. Installation of the EAE adds an 18-bit register, the Multiplier Quotient Register (MQ) to the computer as well as a 6-bit step counter register. The contents of the MQ register are continuously displayed on the operator's console just below the accumulator indicators.

The Type 177 and the basic computer cycle operate asynchronously, permitting computations to be performed in the minimum possible time. Further, since the EAE instructions are microcoded, several operations can be performed by one instruction, thus simplifying associated programming. Average multiplication time is 6.1 μsec, average division time is 9.1 μsec.

Automatic Priority Interrupt Type 172 increases the capacity of the PDP-7 to handle transfers of information to and from input/output devices. The 172 identifies an interrupting device directly, without the need for flag searching. Multi-level interrupts are permissible where a device of higher priority supersedes an interrupt already in process. These functions increase the speed of the input/output system and simplify the programming. More and faster devices can therefore be serviced efficiently.

The Type 172 contains 16 automatic interrupt channels arranged in a priority chain so that channel 0 has the highest priority and channel 17_8 has the lowest priority. The priority chain guarantees that if two or more in-out devices request an interrupt concurrently, the system grants the interrupt to the device with the highest priority. The other interrupts will be serviced afterwards in priority order.

Memory Parity Option Type 176 Provides hardware for generating and storing parity on transfers to memory and checking parity on transfers from memory. It extends each core memory word from 18 to 19 bits.

PROGRAMMING SYSTEM

The PDP-7 Programming System includes an advanced FORTRAN Compiler, a Symbolic Assembler, Editor, DDT Debugging System, Maintenance routines and a library of arithmetic, utility and programming aids developed on the program-compatible PDP-4. Both the Editor and DDT are designed to allow symbolic debugging and computer-aided editing to replace the tedious manual equivalent. New and updated programs are being developed continuously in the applied programming department.

Symbolic Assembler lets the programmer code instructions in a symbolic language. The assembler used on the PDP-7 allows mnemonic symbols to be used for instruction codes and addresses. Constant and variable storage registers can be automatically assigned. The assembler produces a binary object tape and lists a symbol table with memory allocations and useful diagnostic messages.

Digital Debugging Tape (DDT) speeds program debugging by communicating with the user in the address symbols of the source language program. Program debugging time is further shortened when using DDT because program execution and modification are controlled from the teleprinter keyboard. For example, to branch to a new location in the program it is only necessary to type the symbolic location name on the keyboard followed by the character, single quote ('). The same symbol followed by the character, slash (/), causes the contents of that location to be typed. By using DDT to insert break points in a program, the programmer can make corrections or insert patches and try them out immediately. Working corrections can be punched out on the spot in the form of loadable patch tapes, eliminating the necessity of creating new symbolic tapes and reassembling each time an error is found.

Symbolic Editor permits the editing of source language programs by adding or deleting lines of text. All modification, reading, punching, etc., is controlled by symbols typed at the keyboard. The editor reads parts or all of a symbolic tape into memory where it is available for immediate examination, correction, and relisting.

FORTRAN Compiler used with the PDP-7 is based on the field-proven FORTRAN II used with PDP-4 and is designed for programming flexibility and operating efficiency. FORTRAN permits the PDP-7 user with little knowledge of the computer's organization and machine language to write effective programs. Programs are written in a language of familiar English words and mathematical symbols. Compilation of the original FORTRAN source program is performed separately from the compilation of associated subroutines. Thus when errors in FORTRAN coding are detected by the compiler diagnostic, only the erroneous program need be recompiled. *PDP-FORTRAN* features include the following:

FIXED POINT CONSTANTS:

1-6 decimal digits absolute value $\leq 131{,}071$

FLOATING POINT CONSTANTS:

10 decimal digits precision. Exponent range $2^{17}-1$ to $-2^{17}-1$.

SUBSCRIPTS:

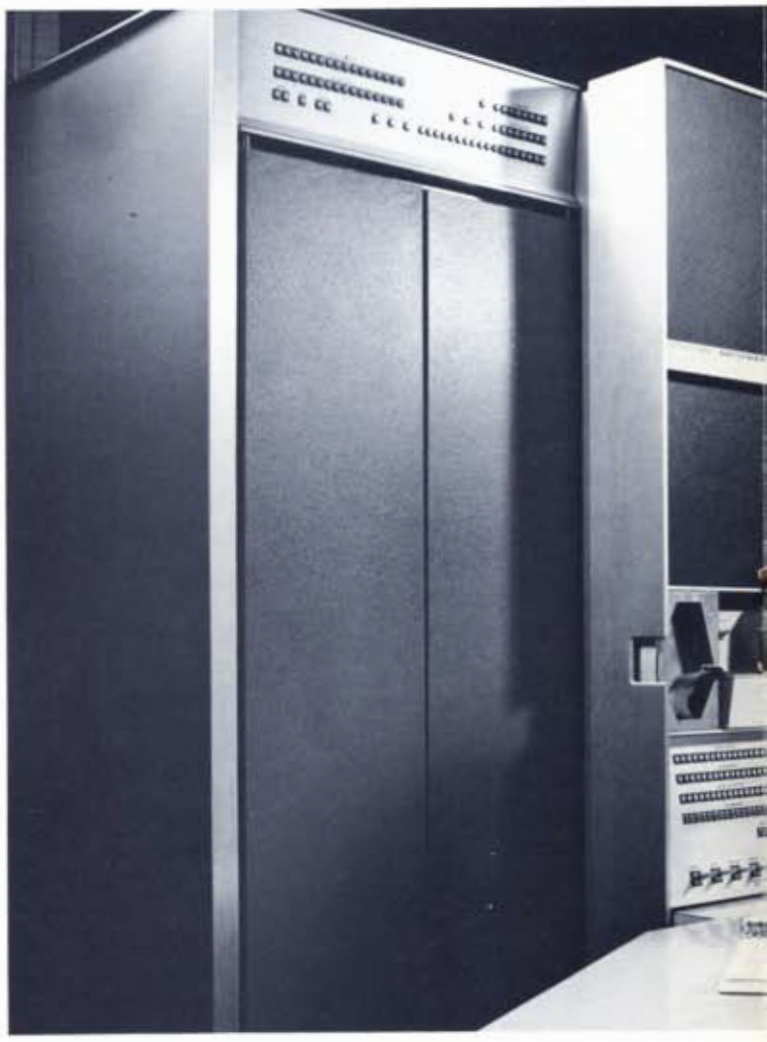
Any arithmetic expression representing an integer quantity: Variables in a subscript may themselves be subscripted to any depth. N dimensional arrays are permitted.

STATEMENTS:

Mixed expressions containing both fixed and floating point variables are permitted. A maximum of 300 characters are allowed (statement numbers not counted).

STATEMENT NUMBERS:

1-99999



FUNCTIONS AND SUBROUTINES:

Subroutines not contained in the FORTRAN library may be compiled by the use of Function and Subroutine statements. Functions and subroutines may be fixed or floating point values as defined by initial letter of F-type function convention. Arguments may be arbitrary arithmetic expressions, including functions.

INPUT AND OUTPUT:

DECtape (Digital's Microtape system), magnetic tape, paper tape, teletype, display. Format may be specified by use of a FORMAT statement.

STATEMENTS AVAILABLE:

Arithmetic statements, I/O statements with FORMAT, DO, Dimension, Common, IF, GOTO, Assign, Continue, Call, Subroutine, Function, Return.

TYPE DECLARATIONS:

Variables may be declared as real, integer, and FORTRAN. Variable names are 1-6 alphanumeric characters.

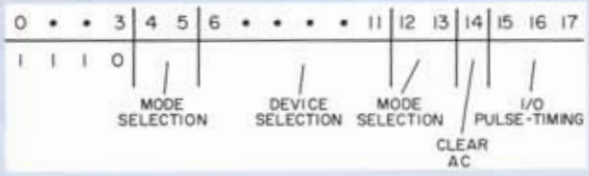
INSTRUCTIONS

Memory Reference Instructions include arithmetic, logical, data handling, and program control instructions. A memory address (bits 5-17) is specified as part of a memory reference instruction. The contents of this memory address are used by the processor in executing the instruction. Bits 0-3 contain the instruction code and bit 4 signifies that the address is to be indirect. Most memory reference instructions require two computer cycles (3.5 microseconds). The first cycle fetches the instruction itself. The second cycle fetches the data addressed and executes the instruction. All memory reference instructions can be executed indirectly.

Operate Class Instructions are microcoded instructions used to shift, skip, and complement. Bits 5-17 specify which operation the processor is to perform when executing the instruction. Each bit location represents a unique operation. For example, a 1 in bit location 5 is the code to clear the accumulator during the execution of the operate instruction. A number of different operations can be performed simultaneously by coding (selecting) several bits in the same instruction.

The Law Instruction loads itself into the accumulator. It provides a means of loading a negative constant without the need of a memory reference to get a stored constant. Two common uses of law are setting up word counts in mag tape transfers and presetting the clock.

IOT (input/output & transfer) Instructions enable the PDP-7 to communicate with external devices, sending control information and transferring data. Certain central processor commands, such as the clock instructions, are also in the IOT class. The IOT instruction is microcoded to simplify programming for I/O transfers. For example, clearing the AC and loading a device buffer are done in one instruction. The ten bits used for device and mode selection provide 1024 possibilities. The format of the instruction is as follows:



RIM: 17763

OBJECT: 17770

MEMORY REFERENCE INSTRUCTIONS

MNEMONIC	OPERATION
CAL Y	call subroutine. Y is ignored jms 20 if bit 4 = 0, jms i 20 if bit 4 = 1.
DAC Y	deposit AC. C(AC) => C(Y)
JMS Y	jump to subroutine. C(PC) => $C(Y_{5-17})$, C(L) => $C(Y_0)$, Y + 1 => C(PC)
DZM Y	deposit zero in memory. 0 => C(Y)
LAC Y	load AC. C(Y) => C(AC)
XOR Y	exclusive OR. C(AC) V C(Y) => C(AC)
ADD Y	add (1's complement). C(AC) + C(Y) => C(AC)
TAD Y	2's complement add. C(AC) + C(Y) => C(AC)
XCT Y	execute.
ISZ Y	index and skip if 0. C(Y) + 1 => C(Y), if C(Y) + 1 = 0, then C(PC) + 1 => C(PC)
AND Y	AND. C(AC) ∧ C(Y) => C(AC)
SAD Y	skip if AC and Y differ. If C(AC) ≠ C(Y), then C(PC) + 1 => C(PC)
JMP Y	jump. Y => C(PC)

OPERATE INSTRUCTIONS

MNEMONIC	OPERATION
OPR	operate
NOP	no operation
CMA	complement, $\overline{C(AC)}$ => C(AC)
CML	complement link, $\overline{C(L)}$ => C(L)
OAS	inclusive OR AC switches C(ACS) V C(AC) => C(AC)
LAS	load AC from switches C(ACS) => C(AC)
RAL	rotate AC + link left one place $C(AC_j)$ => $C(AC_{j-1})$, C(L) => $C(AC_{17})$, $C(AC_0)$ => C(L)
RCL	clear link, then ral. 0 => C(L), then ral
RTL	rotate AC left twice. Same as two ral instructions
RAR	rotate AC + link right one place. $C(AC_j)$ => $C(AC_{j-1})$, C(L) => $C(AC_0)$, $C(AC_{17})$ => C(L)
RCR	clear link, then rar. 0 => C(L), then rar
RTR	rotate AC right twice. Same as two rar instructions
HLT	halt. 0 => RUN
SZA	skip on zero AC. Skip if C(AC) = positive zero
SNA	skip on non-zero AC. Skip if C(AC) ≠ positive zero
SPA	skip on positive AC. Skip if $C(AC_0) = 0$
SMA	skip on negative AC. Skip if $C(AC_0) = 1$
SZL	skip on zero link. Skip if C(L) = 0
SNL	skip on non-zero link. Skip if C(L) = 1
SKP	skip, unconditional. Always skip
CLL	clear link. 0 => C(L)
STL	set the link. 1 => L
CLA	clear AC. 0 => C(AC)
CLC	clear and complement AC. −0 => C(AC)
GLK	get link. 0 => C(AC), C(L) => $C(AC_{17})$
LAW N	load AC with law N, where N equals a constant. law N => C(AC)

EAE INSTRUCTIONS

MNEMONIC	OPERATION
EAE	basic EAE command — no operation
LRS	long right shift
LRSS	long right shift, signed
LLS	long left shift
LLSS	long left shift, signed
ALS	accumulator left shift
ALSS	accumulator left shift, signed
NORM	normalize: max. shift is 44
NORMS	normalize, signed
MUL	multiply unsigned
MULS	multiply signed
DIV	divide C(AC and MQ) as a 36-bit unsigned number
DIVS	divide C(AC and MQ) as a 34-bit 1's complement signed number
IDIV	integer divide unsigned
IDIVS	integer divide, signed
FRDIV	fraction divide unsigned
FRDIVS	fraction divide, signed
LACQ	replace the C(AC) with the C(MQ)
LACS	replace the C(AC) with the C(SC)
CLQ	clear MQ
ABS	place absolute value of AC in the AC
GSM	place AC sign in link and take absolute value of AC
OSC	inclusive OR the SC into the AC
OMQ	inclusive OR AC with MQ and place results in AC
CMQ	complement the MQ

PRIORITY INTERRUPT INSTRUCTIONS

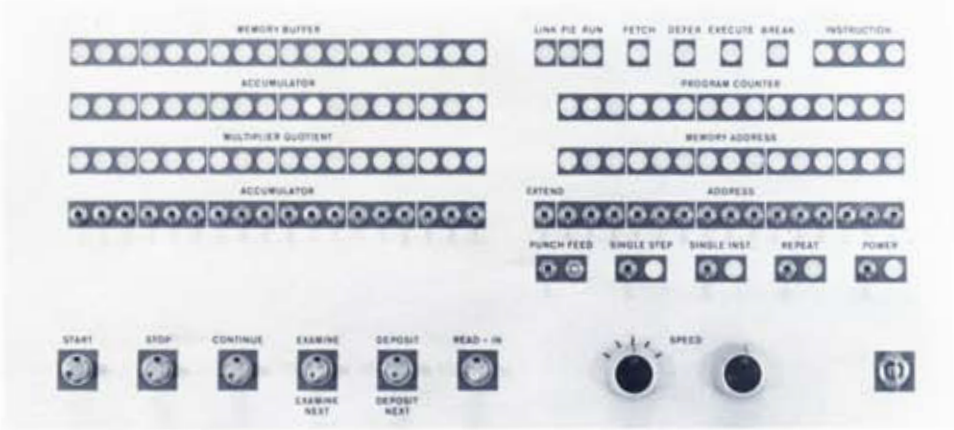
MNEMONIC	OPERATION
CAC	clear and reset all channels
ASC	enable selected channel(s)
DSC	disable selected channel(s)
EPI	enable automatic priority interrupt system
DPI	disable automatic priority interrupt system
ISC	initiate break on selected channel (for maintenance purposes)
DBR	debreak . . . Returns highest priority channel to receptive state

IOT INSTRUCTIONS

MNEMONIC	OPERATION
	Program Interrupt
IOF	turn off interrupt
ION	turn on interrupt
ITON	turn on trap, also turns on program interrupt
	IO Equipment
IORS	read status of io equipment
	Clock
CLSF	skip if clock flag is 1
CLOF	turn off clock, clear clock flag
CLON	turn on clock, clear clock flag
	Paper Tape Reader
RSF	skip if reader flag is a 1
RSA	select reader for alphanumeric, clear reader flag
RSB	select reader for binary, clear reader flag
RRB	read the reader buffer into AC, clear reader flag
	Paper Tape Punch
PSF	skip if punch flag is a 1
PLS	punch a line in alphanumeric mode
PCF	clear punch flag
PSB	punch a line in binary mode
	Keyboard Input from Teleprinter
KSF	skip if keyboard flag is a 1
KRB	read the keyboard buffer into the AC, clear keyboard flag
	Teleprinter
TSF	skip if teleprinter flag is a 1
TLS	load teleprinter buffer and select, clear teleprinter flag
TCF	clear the teleprinter flag

MNEMONIC	OPERATION
	DECtape 550
MMRD	Read. Transfers one word from data buffer to the AC
MMWR	Write. Transfers one word from the AC to data buffer
MMSE	Select. Connects the unit designated to the DECtape control
MMIC	Load Control. Sets the DECtape control to the proper mode and direction
MMRS	Read Status. Reads the DECtape status conditions into bits 0-8 of the AC
MMDF	skip on DECtape data flag
MMBF	skip on DECtape block end flag
MMEF	skip on DECtape error flag
	Tape Control 57A
MSCR	skip if the tape control ready (TCR) level is 1
MCD	disable the TCR flag from the program interrupt and clear command register
MTS	disable the TCR flag from the program interrupt, turn off the WCO flag and EOR flag, and select the unit, the mode of parity, and the density from the AC
MSUR	skip if the tape transport is ready (TTR)
MTC	place AC bits 9-12 in the tape control command register and start tape motion
MNC	terminate the continuous mode (the AC is cleared)
MSWF	skip if the WCO flag is a 1
MDWF	disable WCO flag
MCWF	clear WCO flag
MEWF	enable WCO flag
MIWF	initialize WCO flag
MRC	switch mode from read compare to read
MRD	switch mode from read to read compare
MSEF	skip if the EOR flag is a 1
MDEF	disable ERF
MCEF	clear ERF
MEEF	enable ERF
MIEF	initialize ERF, clear and enable
MTRS	read tape status bits into the AC
MCC	clear CA and WC
MCA	transfer AC bits 5-17 to CA and clear CA and WC
MWC	transfer AC bits 5-17 to WC
MRCA	transfer CA bits 5-17 to AC bits 5-17
	Display 340
IDVE	skip if vertical edge is encountered
IDHE	skip if horizontal edge is encountered

MNEMONIC	OPERATION
IDSI	skip on stop interrupt
IDSP	skip on light pen interrupt
IDRA	read display address
IDRS	clear the light pen flag, restart display
IDLA	load display address, start display
IDRC	read x and y registers
IDCF	clear all flags
IDRD	restart display
	Card Readers
CRSF	skip is reader character flag is a 1
CRSA	select card reader for alphanumeric
CRSB	select card reader for binary
CRRB	read card column buffer into AC
	Line Printer 647
LSDF	skip if the done flag is a 1
LSEF	skip if the error flag is a 1
LPCB	1. clear the done flag 2. clear and initialize the printer buffer 3. set the done flag
LPCF	clear the done flag
LPL1	1. clear the done flag 2. load character C from the AC into the printer buffer 3. set the done flag
LPL2	1. clear the done flag 2. load character B and then character C from the AC into the printer buffer 3. set the done flag
LPL3	1. clear the done flag 2. load character A and then character B and then character C from the AC into the printer buffer 3. set the done flag
LPPB	1. clear the done flag 2. print the contents of the printer buffer 3. clear and initialize the printer buffer 4. set the done flag
LPLS	1. clear the done flag 2. space according to the space channel number in bits 15-17 of the AC 3. set the done flag
LPPS	1. clear the done flag 2. print the contents of the printer buffer 3. clear and initialize the printer buffer 4. space according to the space channel number in bits 15-17 of the AC 5. set the done flag



INPUT-OUTPUT OPTIONS

BLOCK TRANSFER DRUM SYSTEM TYPE 24 Drum transfers operate through the computer's data interrupt facility permitting interlaced program and drum transfer operation. Storage capacities of 32,768 words, 65,536 words, or 131,072 words are available.

PRECISION CRT DISPLAY TYPE 30D Plots data point by point on a 16-inch cathode ray tube in a raster 9⅜ inches square having 1024 points on a side. Separately variable 10-bit X and Y coordinates. Includes program intensity control. Plotting rate is 35 microseconds per point.

PRECISION INCREMENTAL CRT DISPLAY TYPE 340 Plots points, lines, vectors, and characters on a raster identical to the 30D. Plotting rate is 1½ microseconds per point in vector, increment, and character modes. Random point plotting is 35 microseconds.

HIGH SPEED LIGHT PEN TYPE 370 Uses fiber optic light pipe and photomultiplier system for fast detection and modification of information displayed on the precision CRT display.

OSCILLOSCOPE DISPLAY TYPE 34 Controls the plotting of data point by point on an X-Y plotting scope such as the Tektronix Model RM 503. Raster size is 1024 x 1024 points.

INCREMENTAL PLOTTER AND CONTROL TYPE 350 Performs high resolution plotting on paper 12 or 31 inches wide at rates of 12,000 or 18,000 points per minute. Plotting increments are 0.005 and 0.01 inch.

CARD READER AND CONTROL TYPE CR01B, CR02A Provides on-line reading of standard punched cards at 100 or 200 cards a minute in alphanumeric or binary codes.

AUTOMATIC LINE PRINTER AND CONTROL TYPE 647 Prints 300 lines per minute, 120 columns per line, 64 characters per column. Includes single line 120 character buffer.

DATA COMMUNICATION SYSTEM TYPE 630 Provides a real-time interface for up to 64 remote typewriter stations for on-line inputs and outputs. Used in message switching, data collecting, and data processing in multi-user applications.

AUTOMATIC MAGNETIC TAPE CONTROL TYPE 57A Controls up to eight tape transports automatically. Provides information transfer through computer's data interrupt facility, permitting interlaced program and tape operation. Controls reading or writing of tape at various rates compatible with IBM, BCD, or binary parity modes.

MAGNETIC TAPE TRANSPORT TYPE 570 Tape motion is controlled by pneumatic capstans and brakes, eliminating conventional pinch rollers, clamps, and mechanical arms. Tape speed is either 75 or 112.5 inches per second. Track density, program-selectable, is 200, 556, and 800 bits per inch. Tape width is one-half inch, with six data tracks and one parity track. Format is IBM compatible. Dual heads permit read-checking while writing.

MAGNETIC TAPE TRANSPORT TYPE 545 Reads and writes IBM-compatible magnetic tape at 200, 556, and 800 bits per inch and 45 inches per second.

MAGNETIC TAPE TRANSPORT TYPE 50 Reads and writes IBM-compatible magnetic tape at transfer rates of 15,000 or 41,700 cps, and 200 or 556 cpi.

DECTAPE TRANSPORT TYPE TU55 A fixed address magnetic tape facility for high speed loading, readout, and on-line program debugging. Read, write, and search speed is 80 inches a second. Density is 375 bits an inch. Each transport has a stroage capacity of 3 million bits. Features phase recording, rather than amplitude recording; redundant, nonadjacent data tracks; and a prerecorder timing and mark track completely compatible with DECtape Dual Transport Type 555.

DECTAPE CONTROL TYPE 550 Controls up to eight Type TU55 DECtape Transports. Searches in either direction for specified block numbers, then reads or writes data. Units as small as a single word may be addressed.

18-BIT OUTPUT RELAY BUFFER TYPE 140 18 spdt relays actuated by computer command for use to directly control or signal external equipment.

DATA INTERRUPT MULTIPLEXER TYPE 173 Provides multiplex control for simultaneous operation of three high-speed devices such as the Type 57A Tape Control or the Type 24 Drum. Maximum combined transfer rate is 570,000 18-bit words per second.

ANALOG-TO-DIGITAL CONVERTER TYPE 138E Transforms an analog voltage to a binary number, selectable from 6 to 12 bits. Conversion time varies, depending on the number of bits and the accuracy required.

MULTIPLEXED ANALOG-TO-DIGITAL CONVERTER TYPE 138E, 139E The Type 139E Multiplexer permits up to 64 channels of analog information to be applied singly to the input of the Type 138E Analog-to-Digital Converter. Channels can be selected in sequence or by individual addresses.

INTER-PROCESSOR BUFFER TYPE 195 Serves as an interface between the PDP-7 and another computer to permit bidirectional data communication between central processors.

The system shown above is designed for studies in man-machine communication and features both multi-user communication options and graphic display units. Options include the Type 340 Precision Incremental CRT Display, the Type 343 Slave Display, and three teletype stations of the Type 630 Data Communications System.

The system shown below is typical of many installations that wish to combine scientific data processing with real-time data collection and display. This system includes DECtape, the Type 34 Oscilloscope Display and high-speed light pen, the Type 545 Tape Transport with 57A Control, and Type CR02A Card Reader. Also contained in bays four and five are analog-to-digital and digital-to-analog converters.

DIGITAL

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