NORTHROP AIRCRAFT, INC.

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MADDIDA

(Preliminary Report)

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INTRODUCTION

MADDIDA (Magnetic Drum Digital Differential Analyzer) is a digital differential analyzer which employs a magnetic drum memory. A prototype model of this computer has been built and has proved to be capable of solving all types of ordinary differential equations and the types of partial differential equations that are solvable on analogue differential analyzers.

MADDIDA consists of three main elements: a memory, a computing center, and a power supply. The memory is an aluminum drum, 8 inches in diameter and 2-1/2 inches in height, the periphery of which has a magnetic coating. Magnetically recorded on this drum are signals from MADDIDA's 22 integrators and clock pulses for synchronizing the operation of the computing center. Eight vacuum tubes mounted around the magnetic wheel amplify and shape the memory signals.

The computing center is made up of 53 vacuum tubes, a matrix of 904 germanium diodes, and a number of associated resistors and capacitors. Of the 53 vacuum tubes, 32 are used as flip-flops, and 12 are used as amplifiers. The remaining 9 tubes enable a bank of neon tubes to be used as a visual readout device. The germanium diodes are used as clampers and gates in the forming of logical signals.

The power supply furnishes voltage-regulated d.c. power at the four voltage levels used throughout the machine. It employs selenium rectifiers and conventional vacuum tube regulating circuits.

The exceptional features of the design of MADDIDA are readily illustrated by MADDIDA's compactness, its simplicity of construction, and its accuracy. The entire computer, including a cooling system, occupies a floor area of only 7 1/2 square feet. The memory and computing center of MADDIDA are housed in a plexiglass case whose volume is only 5 1/2 cubic feet. MADDIDA's size contrasts sharply with that of an analogue computer, which, if it contained the same number of integrators, would fill a large room.

A total of less than 600 man hours were required for the construction of MADDIDA. This is far less than the amount of work that would be required for the construction of an analogue machine of similar capacity.

The extreme accuracy of MADDIDA results from the 22 binary digit (6 decimal place) capacity of each of its integrators. The ultimate capacity of a mechanical machine is 4 decimal places, and this falls off as the moving parts wear with use.

COMPUTER INTEGRATION

Before describing MADDIDA in detail, it is necessary to explain the general process of computer integration and the particular process of integration employed by MADDIDA.

The fundamental integrating unit of a differential analyzer must satisfy the following requirements:

(1) It must receive two independent inputs of varying magnitudes and produce from them one output of varying magnitude.

(2) It must relate changes in the values of the two inputs and of the output by the equation

$$dZ = K\, dX \sum dy$$

where K is a constant associated with the integrator, and dx, dy, and dz are the changes in the two inputs and the output, respectively. Since y is the accumulation, or sum, of the dy's, this equation can be expressed more simply as

$$dz = K y\, dx$$

(3) The two inputs and the output of the integrator must be expressed in the same form.

(4) This form must express the sign as well as the magnitude of these quantities.

All of the above requirements are satisfied by the wheel-disk integrator, figure 1, which is used in mechanical differential analyzers. In this integrator, the inputs, x and y, and the output z are expressed in the form of shaft rotations. The magnitudes and signs of these quantities are represented by the amounts and directions of rotation. Increments dx, dy, dz, of these quantities are represented by increments of rotation. Since the vertical wheel is positioned by a lead screw which is driven by dy, y is the sum of the initial position of the wheel and the change in the position of the wheel produced by the accumulation of the dy's. It can be seen that for an increment of rotation, dx, of the large wheel, the increment of rotation, dz, of the output shaft can be expressed by the equation

$$dz = K y\, dx$$

where K is determined by the relative sizes of the two wheels.

The type of integrator used in MADDIDA is shown in figure 2. It consists of two accumulators, Y and R, and a transfer device, T. The accumulators could very well be electronic counters. The quantity y in Y is an accumulation of the dy pulse inputs. If for every dx pulse applied to T, y is added to R, and if the dz outputs are the overflows from R, it is apparent that the rate of dz pulses out is equal to Kydz. The constant K is determined by the counter's capacity, which in turn is determined by the point at which the counter is tapped.

The concept of sign is introduced by establishing a fixed pulse rate and then considering the presence of a pulse as representing a positive unit and the absence of a pulse as representing a negative unit. The presence of a pulse in dy adds one unit to the number in the Y counter, and the absence of a pulse subtracts one unit from the number in the counter. Similarly the presence of a pulse in dx adds y to R, and the absence of a pulse subtracts y from R. The dz output represents (1) zero, if it is alternately pulse and no pulse, (2) a positive quantity if it contains a greater number of present pulses than absence pulses, and (3) a negative number if it contains a greater number of absent pulses than present pulses.

Actually, MADDIDA does not employ counters as accumulators. Instead, it holds the R and Y quantities in a magnetic memory, where they are recorded in two channels and are available for transfer operations serially. Thus, only one computing section is necessary; consequently, only a small number of vacuum tubes are required by the computer.

MADDIDA'S MEMORY

Four channels of data are recorded on the magnetic drum of MADDIDA. Three of these are used for temporary storage, being recorded, erased, and recorded again each time the drum revolves. The fourth channel is permanently recorded and contains 1300 equally spaced clock pulses.

The three temporary channels are called the R channel, the Y channel, and the Z channel. They perform the function of R, Y, and Z registers of Figure 2.

The R and Y channels are divided into sections. A separate section on each channel is allotted to each of the 22 integrators. The first half of each section (pulses 1 to 24) is used to hold permanent coded information which controls the transfer of data from one integrator to another. The second half of each section (pulses 25 to 48) is used to hold numerical data for R and Y. This data is operated on once for each revolution of the drum. (See figure 3.)

The code half of each section prepares the computing center for the operations that are to be performed on the numerical data that follows: Control signals for doing this are produced by a coincidence of pulses on the code sections of the R and Y channels in accordance with information obtained from all integrators during the past revolution of the memory. This latter information is held temporarily in a precession line, which essentially shifts the information one pulse space for each integrator period as the memory drum progresses. It is eventually lost, being replaced by new information during the next revolution of the memory. The portion of the R channel of any integrator from pulse position 1 through pulse position 22 is reserved for a dx code pickup pulse. The computer is designed so that only one dx code pulse enables a dz output from one

specific integrator to be fed into the integrator in which the dx pulse is recorded. This dz output is held in a dx register and is used in the computation time of the subsequent, numerical portion of the R channel. Pulse positions 23 through 24 are left blank in the R. channel.

The first pulse space used in the numerical portion of R contains the least significant digit of the R number. This digit occupies the same pulse position as the least significant digit of the Y number. In the type of digital integration used, y is added or subtracted once for each revolution of the drum depending on whether the coded dz output is 1 or 0. Depending on the scale factor used, this least significant digit may be anywhere in the interval between pulse positions 25 and 46. Pulse position 47, of course, contains the most significant digit of the number recorded in R. Pulse position 48 is left blank, but the digit occupying this pulse position in the R + Y adder is recorded in the Z line (precession line) as a dz output from this integrator. This digit governs the sign of the dz output (a one in this position reverses sign).

The Y code occupies the same pulse positions as the R code. The Y channel differs in operation from the R channel since it may be coded to receive dz output signals from as many as seven integrators. These dz outputs are stored as they are picked up during the code period in the dy counter. Pulse position 23 of the Y channel is left blank.

A start pulse preceeds the Y number and occupies the pulse position adjacent to the least significant digit of Y. The start pulse, being the first pulse after pulse position 23 of the integrator, sets a start flip-flop, S, which allows the computing center to operate upon the digital numbers contained in the pulse positions to follow. Thus the start pulse sets the numerical length of a given integrator section. The operations controlled by the start pulse are the addition or subtraction of Y into R and the addition or subtraction of $\sum$ dy into Y. Pulse position 47 controls the sign of the Y number. A pulse in this position gives the number in the preceeding pulse positions a positive sign. Pulse position 48 is always blank.

The Z channel is different from the other memory channels in that it is a general memory storage. Specific portions of the R and Y channels contain information pertaining to given integrators, while the Z channel contains overflow information from all integrators. This information, in turn, is available to all integrators. The length of the Z memory is 49 pulses. This is one pulse time longer than an integrator section. The Z line may take on configurations of 47, 48 or 49 pulse lengths during filling operations.

Since the Z line is one pulse longer than an integrator section and since it records information synchronized at pulse position 48 of each integrator section, the precessing operation of this channel allows information from successive integrators to be recorded adjacently as the memory turns. All dz information for one revolution of the memory is contained in the Z channel. Because of the precessing action, as this information is passed out the read end of the Z line to be recorded, the precessed dz output for a given integrator is made available to any other integrator at a definite pulse time. This pulse time is determined by the relative positions of these two integrators as they have been recorded around the memory. Because of precession this information is available one pulse position later for each subsequent integrator.

The division of the R and Y channels is indexed, as shown in figure 4, by two counters P and I. Clock pulses from the fourth channel of the magnetic drum are fed to the P counter, which has a capacity of 48 pulses. Since this is the same capacity as is allotted to each of the integrators, the P counter produces an output pulse every time an integrator section has passed under the magnetic recording and reading heads of the R and Y channels. The output pulses from the P counter are stored in the I counter, which has a capacity of 22 pulses, corresponding to the total number of integrators. A pulse on the R or Y channel may be found by observing the coincidence between the pulse and the readings of the P and I counters. The reading of the counter I indicates the integrator section in which the pulse lies, and the reading of the counter P indicated the position of the pulse in the integrator section.

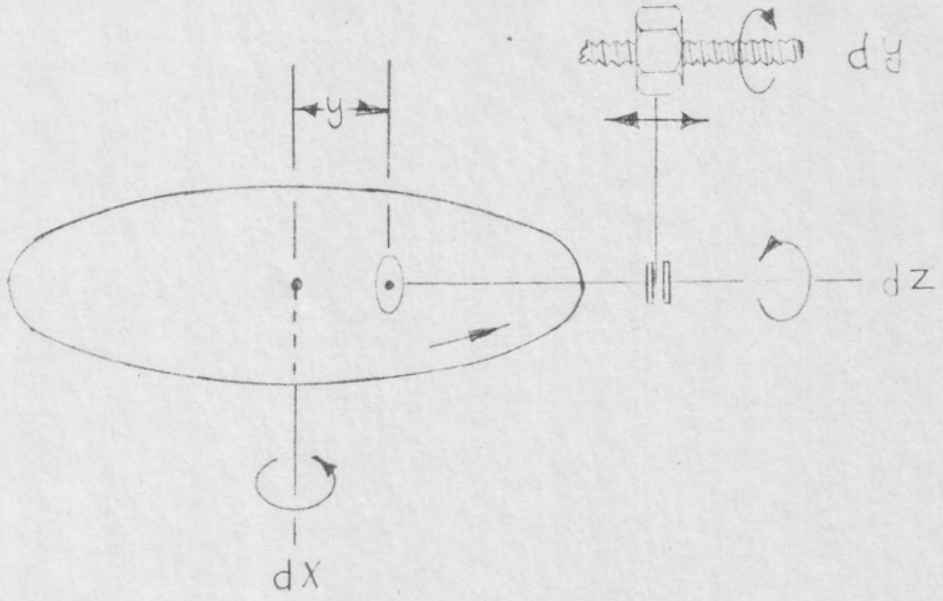


FIGURE 1

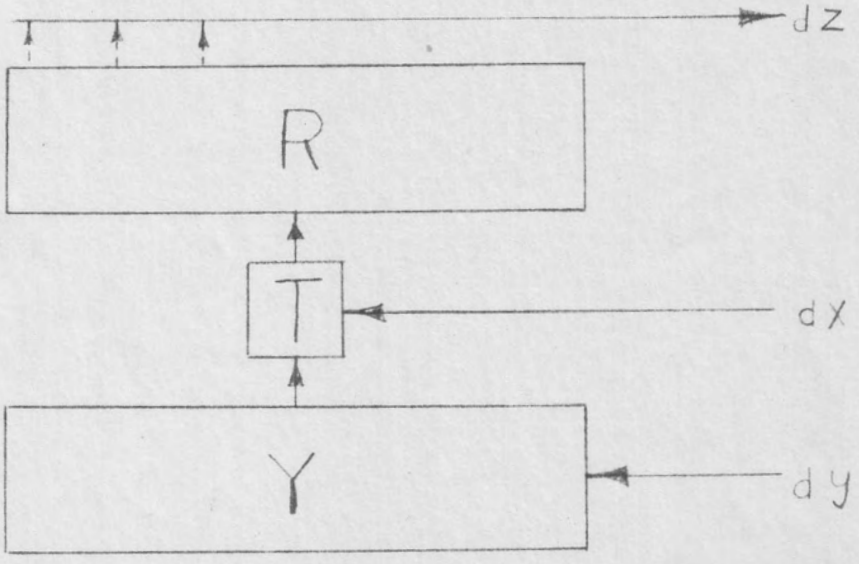


FIGURE 2

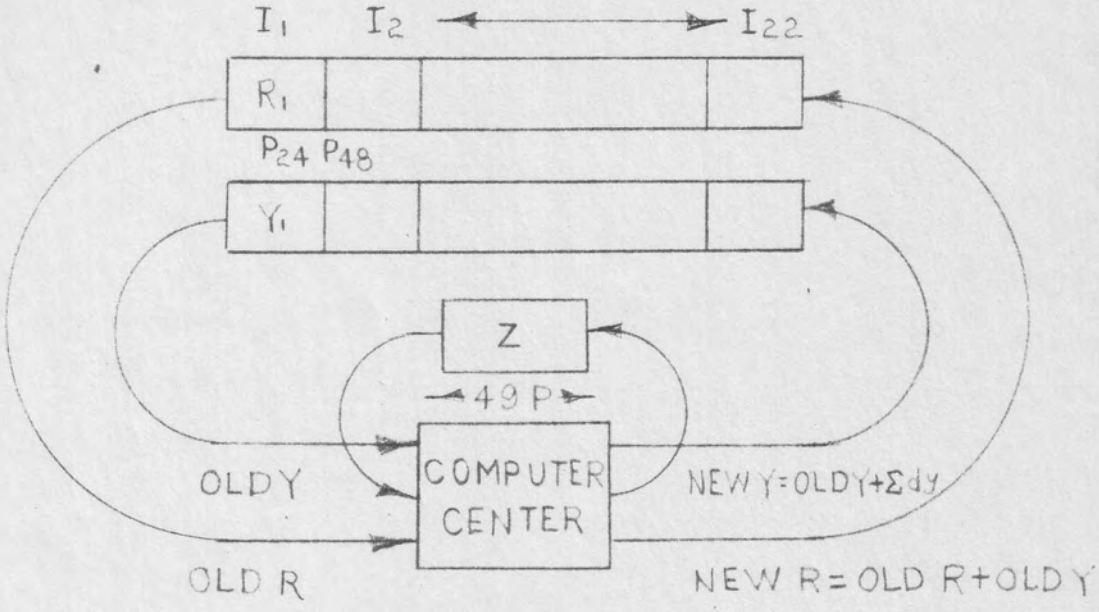


FIGURE 3
THE FLOW OF INFORMATION THROUGH MADDIDA

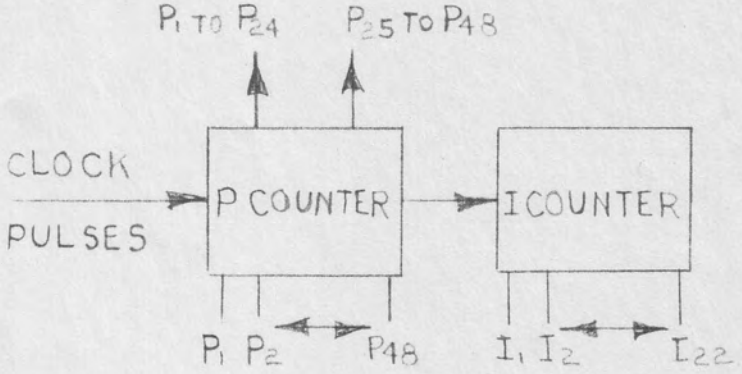


FIGURE 4
CLOCK PULSE INDEXING COUNTERS

MADDIDA'S COMPUTING CENTER

The block diagram of MADDIDA is shown in figure 6. The coded information of the R channel, as it leaves the memory, is gated into the R channel decoder by gate G2. Here, it is compared with the Z channel. At the time corresponding to the code pulse in R, the coincident information of Z is placed in the dx register. If z is one, the dx register sets up a signal, dx^+, which allows Y to be added to R. If z is zero, the signal, dx^-, enables the compliment of Y to be added to R.

The coded section of Y, passes through gate G4. It and the Z channel are decoded, as was R. The coincident signal from Z is added, if it is one, and subtracted if it is zero. After the start pulse, the resulting number in this counter is added to Y.

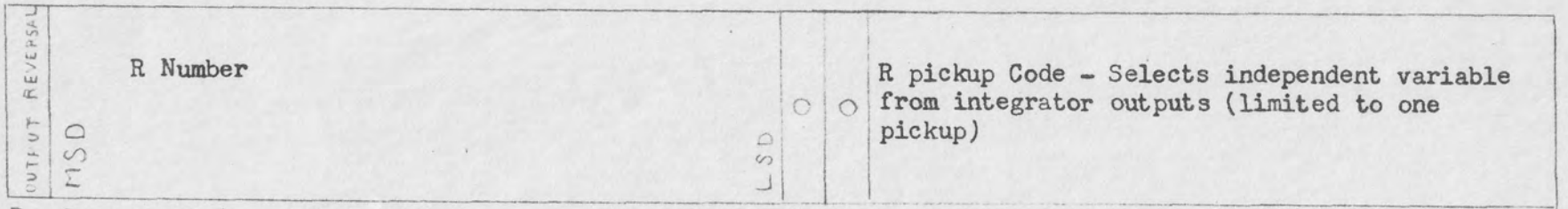
The information in the Z channel is recirculated, except for the pulse in position 48, which closes recirculation gate G5, and opens gate G6, which allows the information in pulse position 48 of R + Y to be recorded in Z.

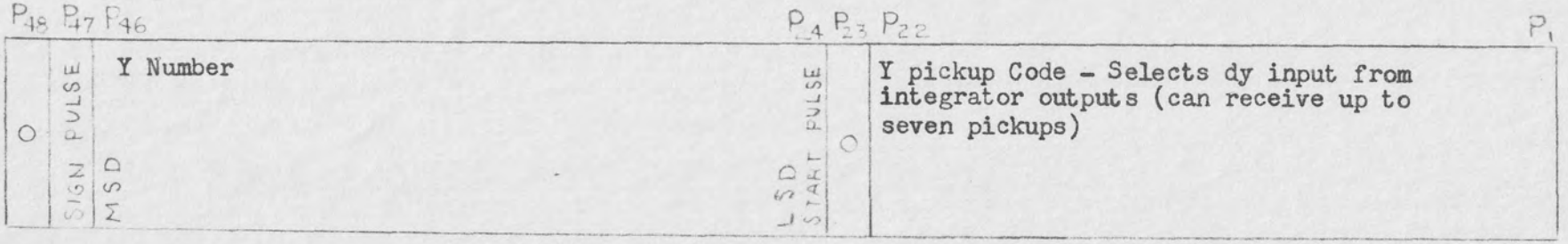
During the second half of the integrator time, the numerical information contained in R is passed through gate G1 into the R + Y adder. Y at this time is passed through gate G3 to the R + Y adder and the $Y + \sum dy$ adder. If the dx^+ signal is present, Y passes through gate G9 into the R + Y adder.

If the dx register is set at dx^-, gate G8 opens and the inverse of the Y signal is sent to the R + Y adder. This inverse signal in conjunction with a signal from D2 produces the compliment of Y. During the computation time, with the exception of pulse position 48, the output of the R + Y adder is recorded in R, and $Y + \sum dy$ is added in Y. At pulse position 48, Y is always zero. Since Y can never have a value of one in pulse position 48, its recirculation records a zero in the memory. Pulse position 48 of R is effectively kept the same by the closing of gate G7 and the opening of gate G10.

The adders $Y + \sum dy$ and R + Y are both serial adders having one pulse delays, D_1 and D_2, for the addition of carry digits. Because of the complementing process, D_2 must have special settings. These are accomplished at pulse position 24. If adding is done, dx^+ and pulse position 24 initially set D_2 at zero. Since the complement of a binary number is obtained by interchanging one's and zero's and adding one to the resulting quantity, an initial setting of D_2 to one at pulse position 24 by dx^- causes the complement of Y to be added to R.

Contents of Y & R Channels





Note: LSD is the least significant digit
MSD is the most significant digit

Start pulse may be placed in any position from P_{24} to P_{25}
LSD of Y and R is pulse position adjacent to start pulse in Y
MSD of R is P_{47}
MSD of Y is P_{46}

Sign pulse of Y: 1 indicates positive number, 0 indicates negative number
Output reversal: 1 gives negative output, 0 gives positive output

Y and R Pickup Code -

P_1 in integrator I_i picks up output of I_i-2

P_2 in integrator I_i picks up output of I_i-3

P_n in integrator I_i picks up output of I_i-(n + 1)

P_{21} in integrator I_i picks up output of I_i from previous revolution

P_{22} in integrator I_i picks up output of I_i-1

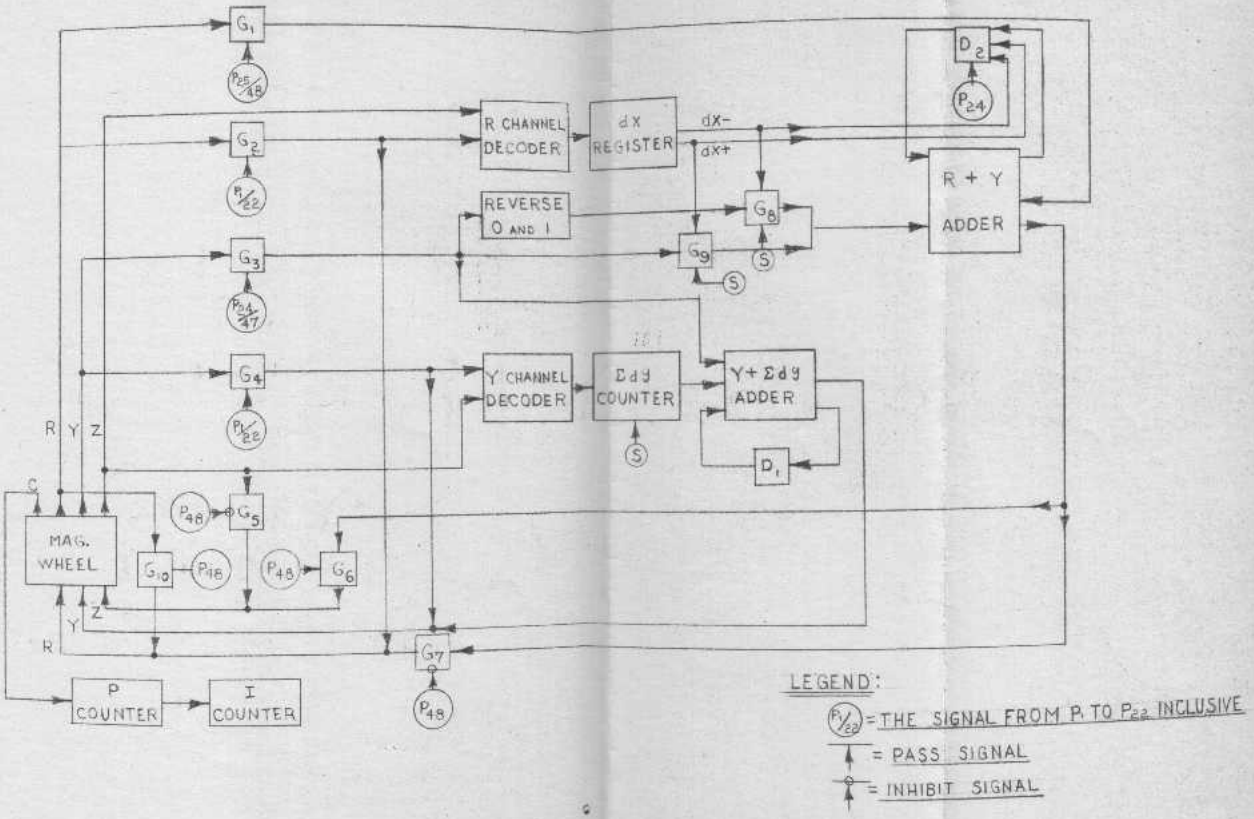


FIGURE 6
BLOCK DIAGRAM OF MADDIDA

MADDIDA's external controls and their functions are listed below.

(1) Operation control switch - This switch has six positions:

- α - Fill Y (the filling process steps right toward the least significant digit with every digit filled).
- β - Fill R (the filling process steps right with every digit filled).
- γ - Step left (this condition steps the pulse position that is available for a subsequent filling condition).
- δ - Step right (this condition steps the pulse position that is available for a subsequent filling condition).
- φ - One operation time (this condition limits computation to one revolution of the memory).
- θ - Compute (this condition gives continuous operation for a predetermined period of the independent variable).

(2) E - Places pulse position 48 in Z line (this gives a reference which controls the filling and stepping operations).

(3) Clear R - Clears the R channel.

(4) Clear Y - Clears the Y channel.

(5) Clear Z - Clears the Z channel.

(6) Sw 1 - Connects Z, R, or Y to the read out.

(7) Sw 2 - Selects first or second half of an integrator time for the read out.

(8) I - A 22- position switch that enables the filling or reading of any one of the 22 integrators.

(9) 0 and 1 buttons - Used to fill 0 or 1 when the computer is in the α, β or E conditions. Either button may be used to step in the γ or δ condition, or to initiate the φ or θ condition.

The operation of the above controls will be better understood when the go flip-flops have been explained. These two flip-flops, G and G_1, enable a signal to appear in the computer when the 0 to 1 buttons are pressed.

As indicated in figure 7, an arbitrary signal from 0 or 1 sets the G_1 flip-flop in the on state. This signal also is applied to a gate which lets the next P_1 pulse of I_1 trigger G. The on signal from G opens a gate, which lets the next clock pulse turn G_1 off, readying it for the next push button signal. When the computer is not in the θ condition, G is turned off after one revolution of the memory. When the computer is in the θ condition, G is turned off after a predetermined increment of the independent variable. This is done by a halt flip-flop, H, which is set by the output pulse of I_1. H then passes the next P_1 pulse of I_1 to turn off G.

Before filling any integrator a pulse from position 48 must be placed in the Z line. After 48 digits have been filled in an integrator, the pulse is lost and must be filled again. This pulse is filled into Z by a gate which is controlled by the E switch and the G flip-flop.

As shown in figure 8 the pulse length recorded on the memory is actually only 46 pulse times. The information read from the memory is passed through a three stage stepping counter, Z, Za, Zb, which makes it available 47, 48, or 49 pulse times removed from the initial record time.

At all times when the G flip-flop is off, the Z line records information from Z_a and recirculates over one integrator time (48 pulse times). When the machine is computing, (i.e. G on in the θ condition), Z_b is recorded and Z precesses over 49 pulse times. In the φ condition, the Z line precesses during the one revolution that G is on. When G is on and the computer is in the α , β , and δ conditions, the Z line precesses over 47 pulse times during the interval, I_i, which is selected by the integrator switch. This shifts the recorded pulse in Z one pulse time earlier (one pulse to the right) with respect to the P and I counters. During the interval I_i for α and β, however, the Z information also is read from Z_a to give the correct time reference in recording the filled digit. In stepping left in the γ condition, the line precesses over 49 pulse times during the interval I_i when G is on. This being the opposite of α , β and δ , the Z pulse is shifted one pulse time later with respect to the P and I counters.

Besides setting G, the 0 and 1 buttons set a flip-flop X. The one button sets it for a one signal, and the zero button sets it for a zero signal. The signal from the X flip-flop is the one that is recorded in filling.

The filling operation is illustrated by the filling of Pi in Y of integrator Ij (See figure 9). Pulse position 48 was initially filled in Z. The number of digits filled in Y up to this point was 48-i. For simplicity it is assumed that the filled digits have all been zero's. The integrator switch has b en set at Ij and the operation switch has been set at α .

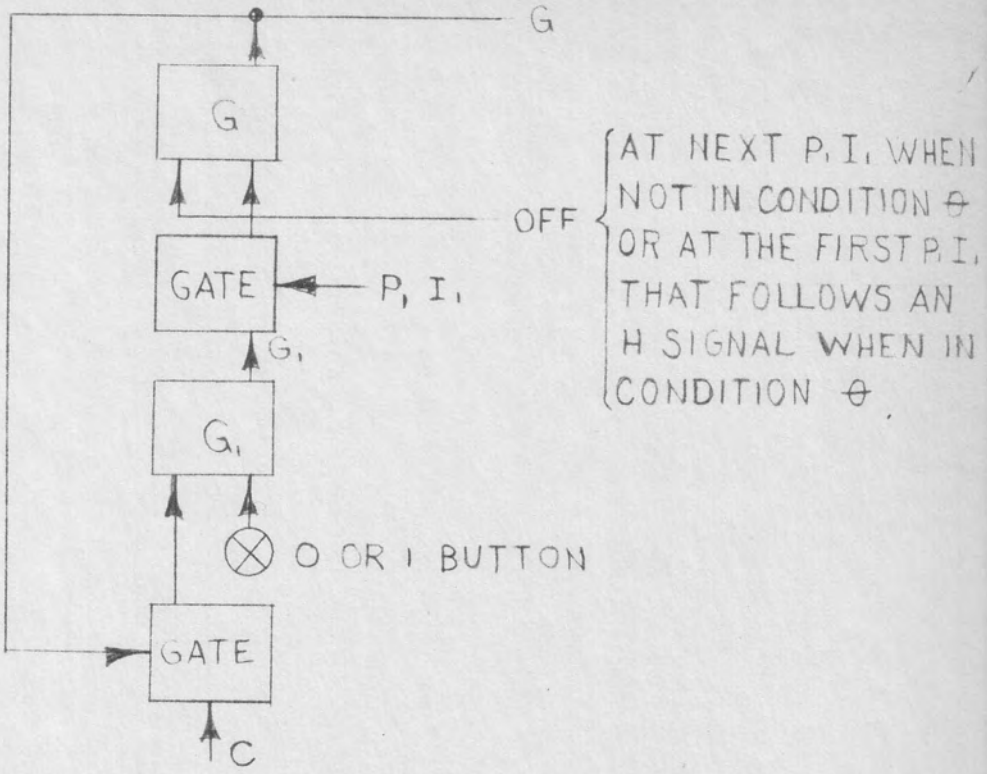


FIGURE 7

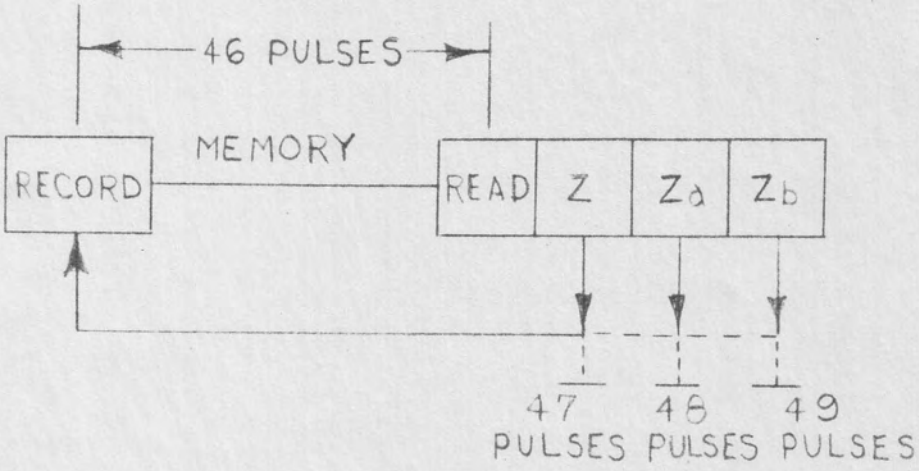


FIGURE 8

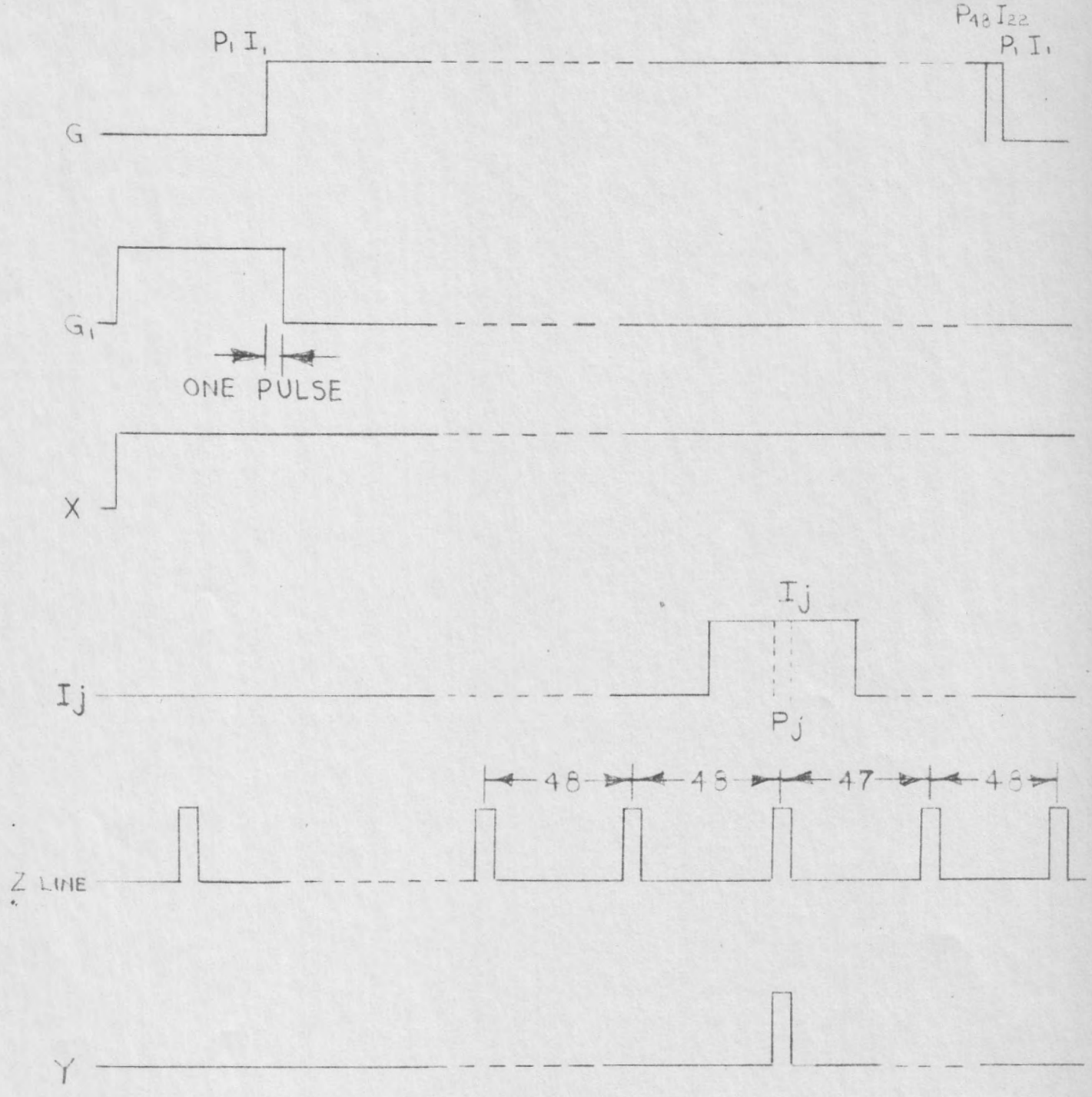

P1 I1
P18 I22
P1 I1
G
G1
ONE PULSE
X
Ij
Ij
Pj
48
48
47
48
Z LINE
Y
1 BUTTON

FIGURE 9

The signal from the one button sets up both the G_1 and X flip flops. X remains in the one state, (until the zero button is pressed), while G_1 is set to zero at $P_2\ I_1$, which is one pulse after G was triggered.

G is turned off after one revolution of the memory. The I_j signal, from the I counter, is zero except during the I_j interval when it is one. The Z line recirculates over a 48 pulse interval until the I_j and G signals are coincident, then it is precessed over a 47 pulse interval for the duration of I_j. It recirculates again after I_j returns to zero. The reference signal from Z is taken from the Z_a flip flop at the time I_j and thus appears at P_iI_j. The coincident signal of G, X, I_j and Z (read from Z_a) is recorded in Y. It is a one in this example; but if the X signal had been zero, the coincidence would be a zero. Since Z has precessed one pulse less than 48 pulses, the coincident signal recorded when the one or zero button next is operated will be a one or zero in the P_{i-1} position of I_j.

The operation in the β condition is the same as the above except that in this condition the information is recorded in the R channel. Operation in the δ condition is similar to that in the condition except that there is no recording of information. The Y condition differs from the δ condition in that Z precesses over a 49 pulse circuit and the Z pulse effectively shifts left.

It has been shown that in the θ condition, G is turned off by a signal from the H flip flop. This is accomplished after the drum has completed a specific number of revolutions fixed by a number set in Y of integrator 1. Integrator 1 differs from the other 21 integrators in that Y is transferred into R once every revolution of the drum. An overflow from R_1 occurs after a time period which is determined by the magnitude of Y. This overflow directly triggers H at $P_{48}\ I_1$. H and G are turned off at the same time, $P_1\ I_1$, of the next revolution.

The logical flip flops of MADDIDA are listed below:

(1) Σ dy counter, A_1, A_2, A_3 and A_4. This counter counts the dy pick up pulses during the code section of an integrator. It has a capacity of $\pm$ 7. After the start pulse in Y, it steps its content into the Y + Σ dy adder. It is cleared to zero after pulse position 48.

(2) dx register, B_5. The setting of this flip flop determines whether Y is added to or subtracted from R. B_5 is set by the coincidence of a pulse in the Z line and a pulse in the code section of R. It exerts control after the start pulse of Y has appeared.

(3) Carry flip flop in the Y + Σ dy adder, D_1. This flip flop delays the carry one pulse in time. Such a delay is necessary in adding two binary numbers in a serial adder.

(4) Carry flip flop in the R + Y adder, D_2. This is also a carry delay for an adder. Ithas an additional feature of adding the extra one to the least significant digit in order to complement the Y quantity.

(5) P counter, F_1, F_2, F_3, F_4, F_5, F_6. The P counter counts sequences of 48 pulses. The first five stages count sequences of 24 pulses by counting to 32 and resetting to 8. The last stage counts the 24 pulse sequences. It has a capacity of two, and produces two output signals, which correspond to the first and second halves of a 48 pulse integrator section.

(6) Go flip flop, G. This flip flop insures that an operation takes place over a determined number of complete revolutions of the memory. It starts and stops between integrators 22 and 1. It is gated on by flip flop G_1. In the θ condition it is gated off by an overflow from I_1 (controlled by the halt flip flop, H). When the computer is not in the θ condition, G is turned off after one revolution of the memory.

(7) Second go flip flop, G_1. This is a manually operated flip flop that controls G. It is initiated by the 0 or 1 button, and is reset by the first clock pulse that comes after G is triggered on.

(8) Halt flip flop, H. H, in conjunction with G, stops computation after a predetermined number of revolutions of the memory. It is set by the overflow from R_1, retains this overflow from P_{48} I_1, to P_{48} I_{22}, and is reset after $P_{48}I_{22}$.

(9) Octal-digit counter, J_1, J_2, J_3, J_4. This counter determines which octal sequence of integrator information will be read out. It also selects banks of three neon bulbs, each of which is controlled by flip flops that store an octal digit (in binary form). In sequences of threes, the neon bulbs flash the information selected by the counter.

(10) I counter, K_1, K_2, K_3, K_4, K_5. This counter counts the integrator sequences of 48 pulses. It has a counting capacity of 22, which it achieves by counting the five stages full at 32 and resetting to 10.

(11) Read-out static register, M_1, M_2, M_3. This is the static register that holds the octal digit selected by the J counter. It lights the neon bulbs in the read-out and holds the information contained in a three-stage stepping counter. The transfer of the latter information is timed by the J counter. M holds all information (taken three binary digits at a time), that passes through the stepping counter. The storage time of M, for each octal digit, is approximately one revolution of the memory.

(12) Last two stages of read-out stepping counter, N_1, N_2. These are the second and third delay states of a three stage stepping counter, which consists of $YN_1 N_2$ or $RN_1 N_2$. These two stages enable the information that passes, one digit at a time, through R or Y to be stored three digits at a time. This information subsequently is transferred to the M register of the read-out. After it has been held for a given length of time, the transfer is repeated for the next three digits of Y or R.

(13) R channel input flip-flop, R. The R flip flop takes information from the R channel memory flip-flop, R_m, and synchronizes it with the clock channel. This is necessary because of the jitter that exists between the R channel and the clock channel. The information in R is available to the computing circuits as it is needed.

(14) R channel memory flip flop, R_m. This flip flop rebuilds the square wave originally recorded on the R channel of the wheel. It does this by appropriate use of the differentiated pulse which is read from the wheel. Since the information read from the memory is a differentiated square wave, the positive pulses trigger R_m to the on state, and the negative pulses trigger it to the off state.

(15) Start flip flop, S. The start flip flop is triggered on by the first pulse in Y after P23, and is triggered off at the end of the clock pulse coinciding with P47. The on signal of S gates the output of the R + Y adder and also gives the signal that calls for Σ dy to be added into Y.

(16) Fill digit flip flop, X. The fill digit flip flop is used for filling. The one button turns it on, and the zero button turns it off. Its setting determines whether a 1 or a 0 is to be recorded in Y or R. The pulse position to be recorded is determined by a coincident pulse in the Z line.

(17) Y channel input flip flop and parallel driver, Y-Yd. This flip-flop performs the same function as the input flip flop in the R channel except that a flip flop, Yd, is used in parallel with it because of excessive loading of this signal.

(18) Y channel memory flip flop, Y_m. The function of this flip flop is the same as that of the R channel memory flip flop.

(19) Z channel input flip flop, Z. The function of this flip flop is the same as that of the input flip flop used in the R and Y channels.

(20) Z channel memory flip flop, Zm. The function of this flip flop is the same as that of the memory flip flop of the R and Y channels.

(21) Z channel delay flip flops, Z_a, Z_b. Z_a and Z_b, in conjunction with Z, form a three-stage stepping counter at the output end of the Z channel of the memory wheel. When it is desired to precess one pulse less than 48 pulse positions, the output signal from Z is used. It provides one pulse time shift in conjunction with each filled digit. For recirculation the signal from Z_a is read back to the Z-record head. This is the normal condition when the computing section is idle. When the machine is computing, the

signal from Z_b is read.

When computation starts, there is nothing recorded in the Z line. Ultimately, the Z line records overflows from the R section's various integrators. These overflows are re-recorded one at a time as integrators pass by. After being carried through one revolution to the original record position they are erased and new information is recorded.

CONCLUSION

MADDIDA is unique among large scale computers because of its compactness, simplicity of construction, and accuracy. A prototype model of MADDIDA required less than 600 man hours for its construction. It occupies only 7 1/2 square feet of floor space, yet it contains 22 integrators capable of six decimal place accuracy. To date, this model has operated for a total of more than 270 hours and for as much as 60 hours without a failure. Transported extensively by air, rail, and truck, it has been consistantly placed in operation within 24 hours after delivery. The performance of this simple model has been remarkable; the potentialities of future models appear unlimited.