TEKTRONIX S-3400 Series Semiconductor Memory Test Systems

TEKTRONIX®
committed to technical excellence

SYSTEMS
DIVISION

A totally new test system concept.

Tektronix semiconductor memory testers transcend the "ordinary" in test electronics design. A completely modular architecture and a data bus interconnect system are used to exploit dramatic new possibilities in digital control and systems organization. Drivers, comparators, timing generators, and more . . . each modularly designed for ready integration into automatic test systems. Today these systems are serving specific needs in the field of semiconductor memory testing.

By combining high-technology design with broad base experience in semiconductor automatic testing, we bring you the S-3400 Series—*the modern family of memory test systems.*

DESIGN GOALS

The S-3400 was designed with the following devices and characteristics in mind:

ROMS—Stored truth table testing. Many bits of storage. 8-bit word organization. MOS and bipolar types.

MOS MEMORIES—One of the most complex circuits produced today. Dynamic and static types with critical timing. A variety of voltage levels. Endless process variations—N, P, SI Gate, CMOS, SOS. Emphasis on functional testing.

BIPOLAR MEMORIES—Fast functional tests required for ECL and TTL. Narrow pulses and precise nanosecond timing. Many DC tests on all pins.

COMPLETE DATA SHEET TESTING

Device manufacturers, incoming device test engineers, quality control inspectors, research and development engineers . . . each with the common problem of "testing", but each with a different point of view and different need. The S-3400 Series does it all.

Capabilities include:

Functional testing with PING PONG, GALLOPING, DIAGONALS, FLOATING, CHECKERBOARD, and many other patterns while setting driver, compare and supply levels to min-max limits.

Proving device performance while operating at specified frequency with 1-ns programmable edges on all signals and strobes.

Testing for worst case pattern sensitivity, access time, timing limits, supply sensitivity, correct logical operation, refresh, cell disturb defects, and cross-related parameters.

DC testing to 80 V at 0.5 A down to 1 mV and 10 nA in either voltage or current supply modes to meet the needs for all types of devices.

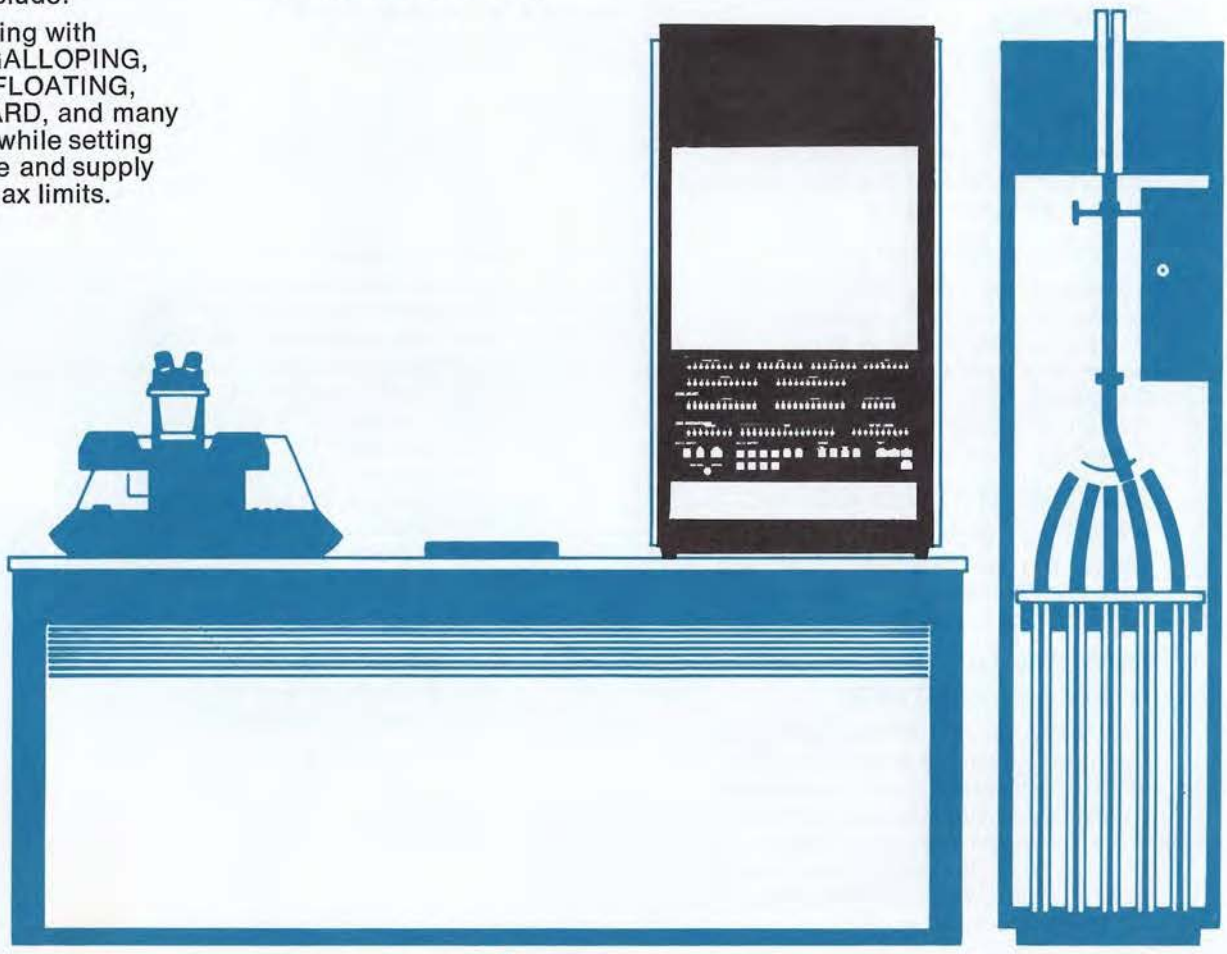
Leakage measurement, input current, output voltage, threshold, protect diode, stress, continuity, and more.

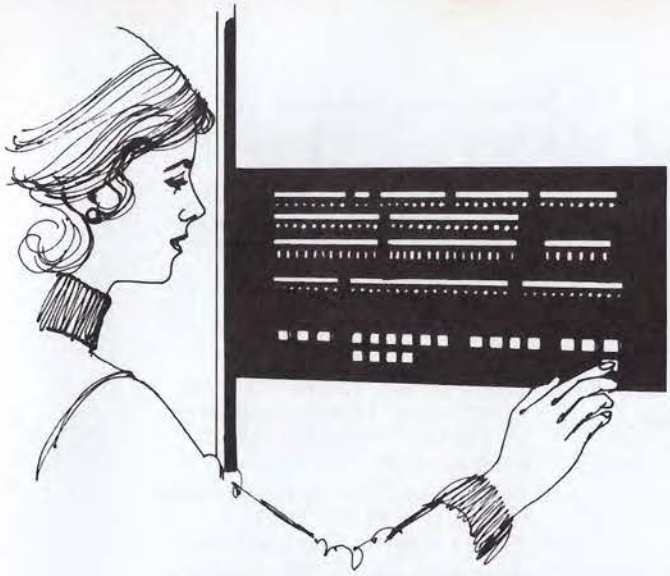
A TEKTRONIX MODEL FOR EVERY NEED

The S-3400 Series family of digitally controlled, stored program systems utilize advanced modular structuring to permit a wide variety of testing capabilities. Each of the four systems is designed to meet specific needs at the most effective cost/performance level possible, yet there are numerous features common to all.

Some common features are:

- A high-speed pattern generator of ECL construction utilizing a 32-bit microcode.
- Programmable tester functions, levels, and timing with no performance cards required.
- Crystal control timing and 1 ns resolution.
- A paper tape reader for program entry, a front panel keyboard for interactive hands-on operation.
- Drivers for ECL, TTL and wide range drivers for MOS.
- Single insertion testing including an AC/DC matrix that fits your prober and handler.
- Optional interface for computer control.
- 256, 512, or 1024-word program control memory.
- Remote sense supplies and DC force/measure unit.
- High reliability and minimum downtime for repair.
- Nationwide on-site maintenance service.
- One year warranty.





OPERATING CONCEPTS

The S-3400 Series uses teletype-compatible paper tape as a permanent storage medium. Since each system contains an RAM stored program capability, with all test parameters programmable, system operation is centered around program loading, hands-on editing and control panel operations.

LOADING THE TEST PROGRAM TAPE . . .

The test program can be loaded directly into the tester for execution or into the control memory for repeated execution.

VERIFYING THE PROGRAM LOAD . . .

If you wish, the contents of the control memory can be verified by single step operation, reading from the instruction display and your listing.

CONTROL SETUP . . .

You select the operating mode(s) needed for your test sequence.
If using an oscilloscope, the sync points you'll need in the pattern may be individually selected.
If volume testing, the "Devices Tested Counters" may be initialized.

PLUG IN THE DEVICE— START TESTING . . .

Plug in the device adaptor card and then the device—the "Continuity" test will verify its connections.

DEBUGGING PROGRAMS & EXPERIMENTING

You may change voltages, timing and test patterns without disturbing the stored program. Simply use the keyboard to edit a voltage, pattern etc. right in the test hardware. After a change is verified simply use the keyboard to store the modified instruction in the control memory.

TEST PROGRAM FOR 1103 DYNAMIC RAM USING GALLOPING PATTERN AT 70 DEGREES C, MIN LIMITS

```
00 * 02 074740 SUPPLY #2 VBB = + 19.50V
01 * 01 062000 SUPPLY #1 VSS = + 16.00V
02 * 04 057640 VH ADDR = + 15.30V
03 * 05 174700 VL ADDR = − 1.00V
04 * 06 057640 VH DATA = + 15.30V
05 * 07 174700 VL DATA = − 1.00V
06 * 10 057640 VH CE,R/W, PCHG = + 15.30V
07 * 11 174700 VL CE,R/W, PCHG = − 1.00V
10 * 12 000360 VH COMPARE = + 30 MV
11 * 13 000240 VL COMPARE = + 20 MV
12 * 40 007200 PERIOD = 580NS, CLOCK 100MHZ
13 * 20 000400 ADDR START = 40NS,NRZ
14 * 21 003600 ADDR STOP = 300NS,NRZ
15 * 22 004500 DATA START = 370 NS,RZ
16 * 23 006700 DATA STOP = 550 NS,RZ
17 * 24 002100 CE START = 170NS,RO
20 * 25 006310 CE STOP = 512NS,RO
21 * 26 004724 R/W START = 395NS,RO
22 * 27 006430 R/W STOP = 526NS,RO
23 * 30 000300 PCHG START = 30 NS,RO
24 * 31 002524 PCHG STOP = 215NS,RO
25 * 32 004310 COMPARE STROBE START (375NS + 23NS)
26 * 33 004644 COMPARE STROBE STOP = 389NS
27 * 51 000000 PAT GEN START LOAD ADDRESS
30 * 52 017411 GALLOPING PATTERN MICROCODE
31 * 52 000760 LOAD INTO PATTERN GENERATOR
32 * 52 031006 7 MEMORY LOCATIONS USED
33 * 52 000000
34 * 52 003576
35 * 52 000004
36 * 52 004201
37 * 52 000024
40 * 52 031421
41 * 52 006002
42 * 52 031006
43 * 52 004002
44 * 52 004624
45 * 52 000054 GALLOPING PATTERN MICROCODE
46 * 70 000000 SELECT PATTERN PROGRAM IN MEMORY
47 * 71 050052 SET ERROR TRAP TO 52
50 * 71 000000 START PATTERN GENERATOR
51 * 72 010053 JUMP TO 53
52 * 71 010000 SET FAIL FLAG
53 * 12 000000 VH COMPARE = OV
54 * 13 000000 VL COMPARE = OV
55 * 04 000000 VH ADDR = OV
56 * 05 000000 VL ADDR − OV
57 * 06 000000 VH DATA = OV
60 * 07 000000 VL DATA = OV
61 * 10 000000 VH CE, R/W, PCHG = OV
62 * 11 000000 VL CE, R/W, PCHG = OV
63 * 01 000000 VSS = OV
64 * 02 000000 VBB = OV
65 * 71 040000 END OF TEST
```

PROGRAMMING

A "Test Program' is a series of digital "instructions," placed in ordered groups, to establish level, timing, pattern and control sequences required to test a device. The S-3400 Series Testers provide the test programmer with the flexibility and system functions normally associated only with large computer-controlled systems. Test programs can include functional and DC parametric tests with a variety of patterns, levels, currents, voltages and frequencies.

PATTERN GENERATION

The programmable test pattern generator provides the functional test patterns required for RAMS, ROMS, and other devices. The pattern is defined by a 32-bit microinstruction executed within the pattern generator at actual functional test rates. The microcode may be loaded as part of the test program, or the test program may use a pattern stored in the ROM Library. Ping Pong, Galloping, and other patterns for 1K word memory chips require six to eight microinstructions. A variety of memory test patterns are provided with the system.

TIMING

The frequency of operation while function testing as well as the precise location of all transition edges and comparator strobe(s) are programmed functions. One binary word programs period and resolution; two binary words program start and stop edges for each timing phase.

LEVELS

Each programmable level provided in the system, such as drivers, comparators, and supplies, is specified by one binary word. The number of programmable levels varies with different system models.

MARGIN CONTROL

To enable memory device testing for guaranteed performance over a specified operating range, a system controller is provided which allows many combinations of voltage and timing settings to be mixed with any or all functional patterns. Such a series of tests with a test program could include continuity, DC parametric and functional tests combined with numerous margin condition tests for device classification.

LANGUAGE

The S-3400 Series Testers are programmed in octal (0 through 7) coded machine language. Each programmable function within the system is assigned a two-octal character code or "instruction' address (6 bits). The data value to be provided with that address may vary from one to six octal characters (one to 16 bits). A programming manual provided with the systems includes sample programs, programming aids and forms, and complete explanation of each "instruction." The tape format permits fully "commented" tapes and listings. The language used by the testers is the same, whether originating from paper tape, the keyboard, or external computer.

PROGRAM TAPE GENERATION

Creation of a paper tape program requires definition of the tests, writing the "instruction" sequence with comments, and punching the tape. After a program is loaded, editing is easily accomplished on the front panel keyboard. The keyboard can also be used for system programming.

TEKTRONIX S-3400 Series Semiconductor Memory Test Systems

S-3420

- A low-cost, general-purpose functional tester for MOS, and TTL memories
- Ideal for incoming inspection and device evaluation
- Complete pattern and timing programmability
- Expandable to an S-3430, S-3440 or S-3450
- Standard test head—patch DUT interconnect

S-3430

- A low-cost, high-speed functional tester especially suited for ECL, CMOS, and TTL memories
- Add DC parametrics to perform all types of tests
- Levels, timing and supplies configured for easy programming of Bipolar devices
- Add comparators to make one-nanosecond time measurements
- fast rise/fall time pulses and edges

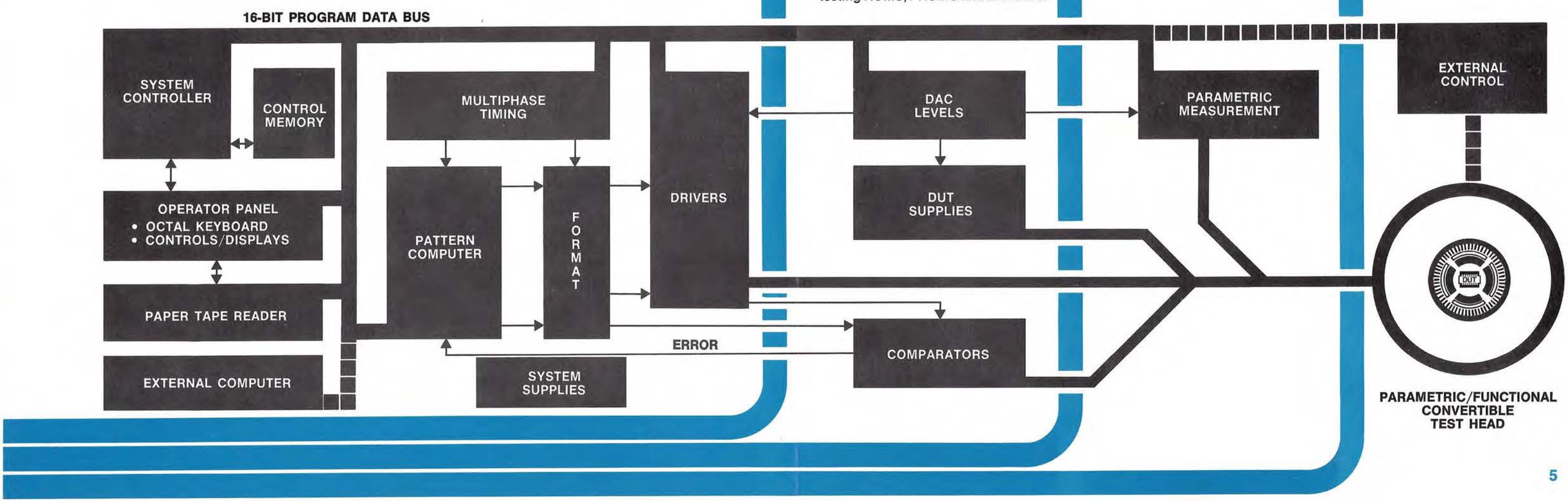
S-3440

- A high-performance functional tester for complex memories
- All functions programmable—drivers, comparators, supplies, timing
- Supplies, levels and timing for MOS and Bipolar memories
- Performs complete functional tests, verifying margin limits on all parameters
- Add truth table pattern option for testing ROMS, PROMS and EAROMS.

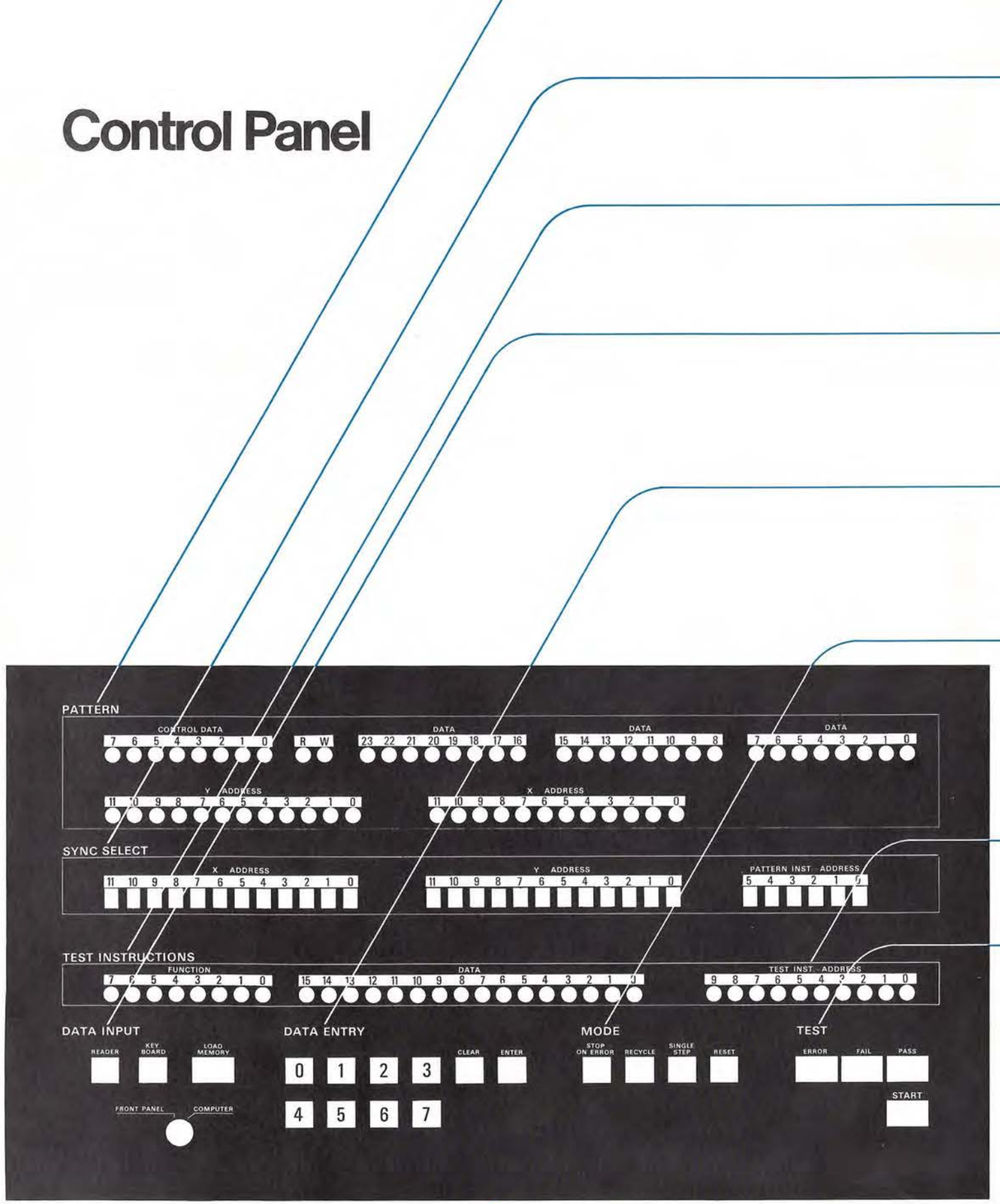
S-3450

- A high-speed functional and DC parametric tester
- Single insertion testing—performs all data sheet tests
- Remote test head/matrix—mounts to wafer probe, autohandler, oven—accepts standard probe card directly
- Driver levels and timing for both MOS and Bipolar memories
- Add truth table pattern option for general-purpose tester use
- Add control for wafer probe, sorter, auto-handler

Functional Block Diagram



Control Panel



PATTERN

CONTROL DATA: LED display of control lines to external equipment.

R (Read), W (Write): LED display of read and write control lines. Shows read, write, and read/write as separate states.

DATA: LED display of pattern generator "Data" lines. Shows actual data word at failed address when stopped on error/fail. "Data" lines are assigned clock gating, chip select, chip enable and functions other than DUT data word bits as required by DUT specifications. Multiple output comparator configurations may use additional data display lights for error display.

X ADDRESS, Y ADDRESS: LED display of pattern generator X and Y address fields. Shows actual address where error occurred when stopped or error/fail.

SYNC SELECT

X ADDRESS, Y ADDRESS, PROGRAM COUNTER: When functional testing, these switches control the occurrence of three different ECL, 100-ohm oscilloscope sync signals available via BNC connectors located on the front lower right-hand corner of the system.

1) **XY Sync**—pulse occurs on coincidence of test pattern output with the state of X, Y address and program counter switches.

2) **Advance Sync**—pulse occurs if program counter advances at the step selected by program counter switches.

3) **Jump Sync**—pulse occurs if program counter jumps at the step selected by program counter switches.

INSTRUCTION

ADDRESS: LED display of the "Address" or tester function code portion of the test program "instruction" register. Two octal characters (6 bits) are displayed when the test system is programmed from paper tape or the keyboard; two additional bits are used when the system is operated from a digital computer. The display is operative when loading, entering, or executing test program instructions.

DATA: LED display of the "Data" portion of the test program "Instruction" register. Up to six octal characters (16 bits) are displayed. The display is operative when loading, entering, or executing test program instructions.

DATA INPUT

READER: Runs paper tape reader and loads ASCII test program tape into the system. If "Load Memory" switch is lighted, the test program will be loaded into the system control memory; if switch is not lighted, the test program will be loaded directly into the addressed tester function.

KEYBD (Keyboard): Selects the program "Data Entry" keyboard as the test programming input source to either the system control memory or addressed tester function. When keyboard is set (lighted), the "Reader" switch is not operative.

LOAD MEM (Load Memory): Selects the system control memory or actual addressed tester function as the location when program data from either the keyboard or paper tape reader will be stored.

DATA ENTRY

Operative only if "keyboard" is lighted.

0 through 7: Loads octal (3 bit) characters into the "Instruction" register. Characters are loaded sequentially starting on the left: two for address and up to six for data, depending on the tester function (number of bits required) being programmed.

CLEAR: Zeros or clears contents of displayed "Instruction" register. Used to correct manual loading errors.

ENTER: Enters contents of displayed "Instruction" into either system control memory at displayed "Memory Address" location or addressed tester function directly, without disturbing control memory contents.

MODE

The normal automatic mode of system operation does not require that any "Mode" buttons be set (lighted). In this mode of operation, test programs are executed until an "Error" condition or end of test ("Pass") occurs. When the next "Test" command is received, the system will initialize itself and start program execution again from the beginning.

STOP ON ERROR/FAIL (Single Step): Causes the test system to stop program execution on any error. The next "Test" command will advance the program to the next error condition or end of test.

RECYC (Recycle): Causes the system to execute the complete test program repeatedly.

S STEP (Single Step): Causes the test system to execute a single "Instruction" or "Pattern" word each time a "Test" is received.

RESET: Resets the test system indicators and returns the system control to initial condition. A "Test" command following will start system operation from the beginning of the test program.

INST ADDRESS

LED display of the binary "Control Memory Address." The number of bits operative varies with amount of control memory installed in the test system: 256, 512, 768, or 1024 words of 22 bits. The number displayed is the specific test program instruction number and the current control memory address. The "Control Memory Address" register may be set to any location via the keyboard, paper tape reader or external computer, permitting a stored test program editing function. A complete test program is a sequence of these instructions.

TEST

ERROR (Red): Displays any go/no-go DC parametric or functional "Error" occurring during the execution of a test program. Since the condition of "Error" may be established via test program instructions as a branch or classification condition not causing a "Fail" state, "Error" is displayed separately from test program "Fail."

FAIL (Red) **PASS** (Green): Displays test program "Pass" or "Fail" condition established at the end of test program instruction execution.

TEST: Starts execution of test program instructions located in control memory. When lighted, the test button indicates a test in progress. In the "Single Step" mode, "Test" advances the "Control Memory Address" register, and when test control is shifted to the pattern generator for a functional test portion of a test program, the "Pattern" output is advanced one step.

Characteristics

DEVICES TESTED

MOS (RAMS, ROMS, PROMS, SR) PMOS, N Channel, and CMOS Levels

BIPOLAR (RAMS, ROMS, PROMS, SR) TTL ECL and High Level Logic

TEST CAPABILITIES

FUNCTIONAL DUT exercised with patterns to 12 MHz. Up to 18 drivers with programmable levels and slew rates of 1 V/ns.

Drivers

Range	Resolution
0 to ± 5V	2.5 mV
0 to ± 15V	10 mV
0 to ± 40V	(consult factory)

Current Output

50 mA dc, 200 mA pulse.

TIMING Propagation delay, response time, hi-low frequency limits, access time, critical timing relationships.

Accuracy	Resolution
± 1 ns	1 ns
± 3 ns	1 ns
± 7 ns	10 ns

DC PARAMETRIC Stress, leakage, threshold, input current, output voltage, protect diode, continuity.

Voltage Force or Measure

Range	Resolution
0 to ± 2V	1 mV
0 to ± 20V	10 mV
0 to ± 80V	40 mV

Current Force or Measure

Range	Resolution
0 to ± 20μA	10 nA
0 to ± 2mA	1 μA
0 to ± 200mA	100 μA
0 to ± 500mA	250 μA

Compliance voltage limiting.

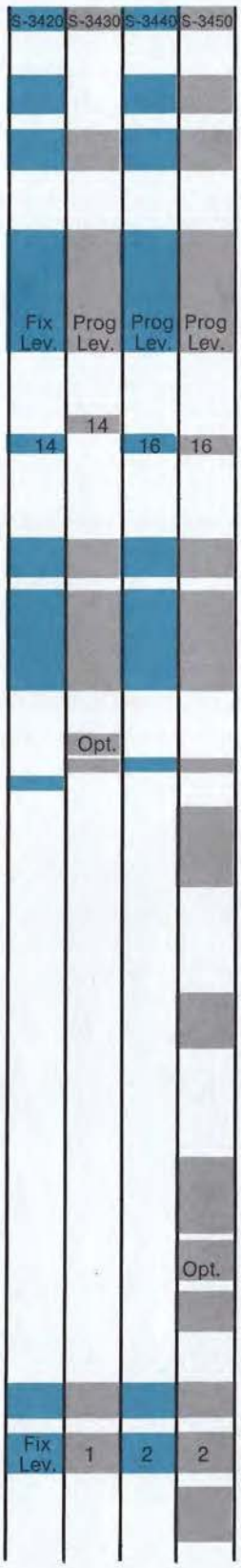
PIN CONTINUITY ± 100 mA applied, measure all pins

LEVEL FORCING

FUNCTIONAL Reverse terminated 50 Ω drivers

DUT POWER Up to 4 supplies, 20V, 200mA, 10 mV rs.

PARAMETRIC Force/measure voltage or current, one pin at a time.



MULTIPHASE CRYSTAL CONTROLLED TIMING

TEST PERIOD 7 Decade Ranges

Frequency Range	Resolution
12 MHz to 100 KHz	10 ns
— down to —	
50 Hz to 0.1 Hz	10 ms

TEST PHASES From 3 to 7 programmable edge increments:

1 ns
10 ns

HIGH-SPEED TEST PATTERN SOURCE

MICROPROGRAM PATTERN GENERATOR The pattern generator provides address and data patterns to 12 MHz.

ADDRESS GENERATOR 8X and 8Y independent

DATA GENERATOR 4 control data lines for chip select, precharge, and clock control; 1 read/write line and 1 data line. Data field expandable to 8 bits in standard system. For data field expansion to 72 bits, consult factory.

RANDOM DATA 10 MHz RAM add-on 16 bits x 512 or 16 bits x 1024 word blocks.

FORMAT NRZ, RZ, or RO

FUNCTIONAL TEST PATTERNS Typical patterns are: Walk data, Ping Pong, Surround Disturb, Adjacent Disturb, Corner Disturb, Bit Complement, Diagonals, Write/Read.

OPERATION AND PROGRAMMING

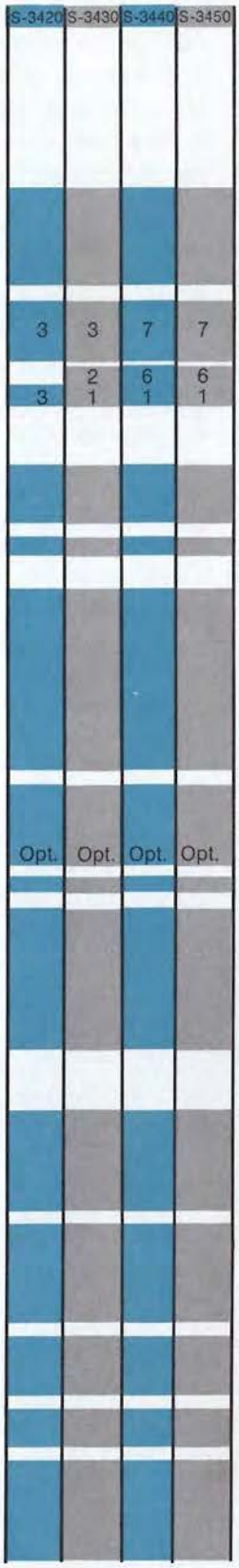
OPERATOR CONTROL Test, Pass/Fail, Error, Stop on Error/Fail, Recycle, Single Step, Reset, Programmed Sync.

PROGRAMMING LANGUAGE Octal coded machine language. A paper tape reader is provided to load ASCII program tapes.

PROGRAM ENTRY Manual panel, paper tape reader, or read-only memory

TEST PROGRAM STORAGE 256 to 1024 words (22 bits).

DISPLAY 8X, 8Y and 24 data indicators show state of DUT pins. Sync pulse setting for oscilloscope viewing.



Business Information

With approximately 11,650 employees and annual sales of over $232 million, Tektronix, Inc. is a recognized leader in the manufacture, sales and service of scientific instruments. Considerable time and effort is continuously devoted to designing and producing a broad line of products which effectively fulfill a wide range of test and measurement needs.

SATISFY YOUR MEASUREMENT REQUIREMENT

Systems Applications Engineers will help you select the product best suited for your present and future needs. Ask him about any product described in this booklet, or for other products described in our general catalog. You will find the address of the Systems Applications Engineer nearest you on the back cover.

PRODUCT SUPPORT

It is our intent to consistently provide unexcelled product service and support at competitive prices.

Your Applications Engineer is fully prepared to respond to your technical and business requirements. He has a strong technical background and extensive product and business training. Constant communication with Beaverton-based technical and software support personnel enables him to remain current on new products and services. Call upon him for assistance any time you have questions about Tektronix, Inc. and its products.

OPERATION

Your Systems Applications Engineer will be glad to demonstrate the TEKTRONIX S-3400 in your measurement environment. Informal classes on product operation can be arranged at your convenience.

ORDERING

An Applications Engineer will provide information on prices, terms of sale, shipping estimates, and best method of transportation for all products, accessories, and replacement parts.

SERVICE

If you require service, replacement parts, a warranty question resolved, or other help, please notify the Tektronix facility through which you ordered your instrument. They will process all orders for repair parts promptly, and provide emergency part[redacted] service when needed to restore an instrument to operating condition. They will also arrange for fast service with necessary recalibration or repair work on your instrument.

TEKTRONIX®
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SYSTEMS DIVISION

☐ **I am interested in seeing your S-3400 Memory Test Systems. Please have my System Applications Engineer contact me.**

☐ **I am interested in automated testing. My application is** _____

Please send me the appropriate literature.

Position _____

Name _____

Address _____

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My phone no. is _____ Area Code _____ Phone

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