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vintageTEK

Tektronix Equipment

Installing and Using the 468 ROM Replacement

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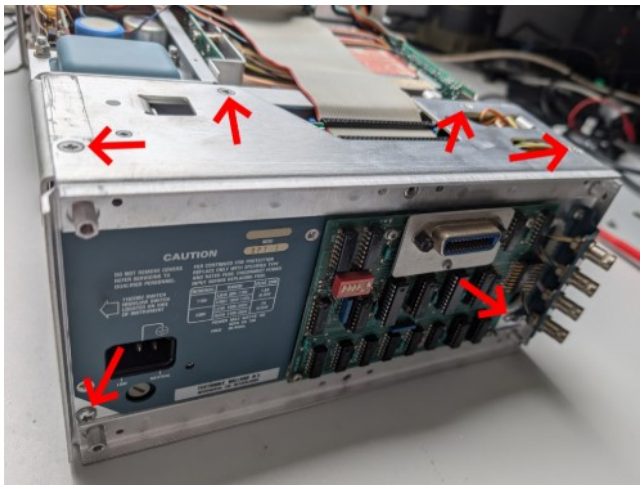
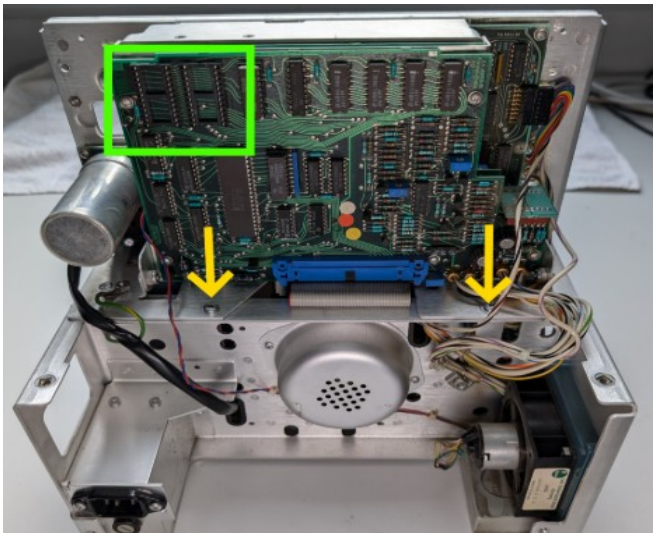
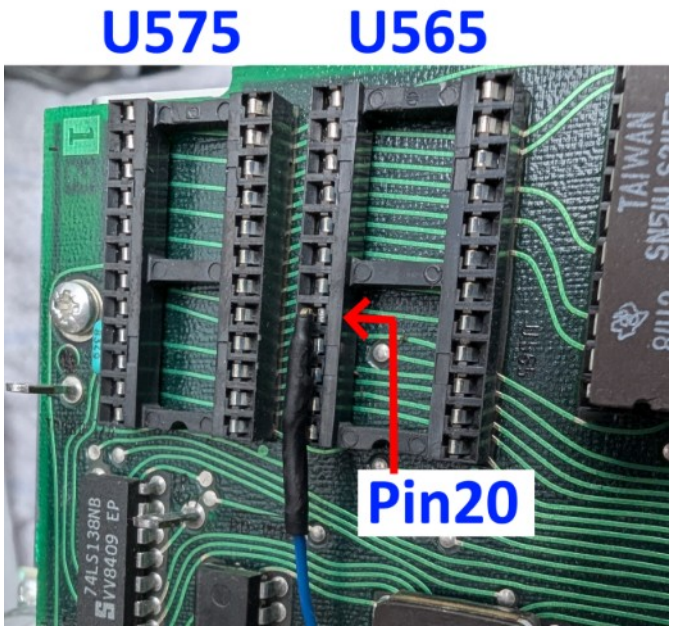
Installation of the new ROM board

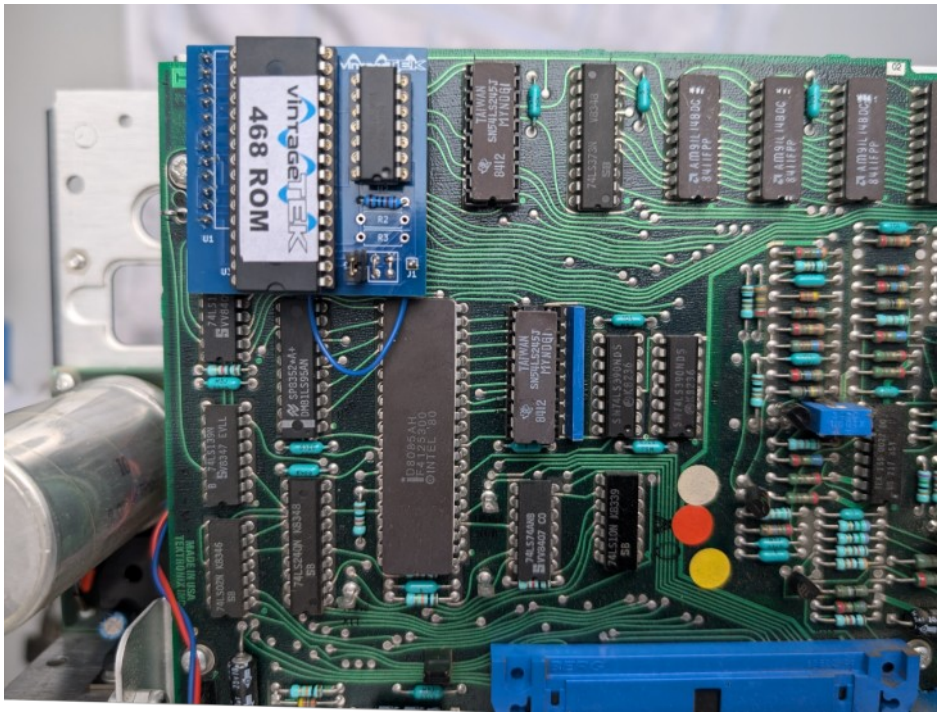
- Unscrew the 4 feet plus the 2 screws holding the rear cover.
- Slide the 468 out of the cover while protecting the front panel
- Unscrew the digital section at the rear of the scope. There are 2 screws at the back and 4 screws on the top – see red arrows in the picture at the right
- Disconnect the ribbon cable between the top board (Storage Display Board) and the digital section on the side of the top board.
- Carefully loose the digital section and flip it over so it sits on top of the 468. But be careful to not pull any wires out of their sockets during this procedure.
- Secure the digital section on top of the 468 with two screws. See yellow arrows in the picture.
- Reconnect the ribbon cable to the top board again.
- The two firmware ROMs are located in the top left of the CPU board. See green rectangle in the picture. U575 is the outermost ROM, U565 is towards the inner side of the PCB
- Remove the two ROM ICs.
- Insert the flying pin of the vintageTEK replacement board into pin 20 of U565.
- Insert the new ROM board in the U575 socket (the one nearest the edge of the board). Orient it as shown in the photo on the next page.







- Ensure the jumper on the new board is closed
- The instrument should now power up correctly.

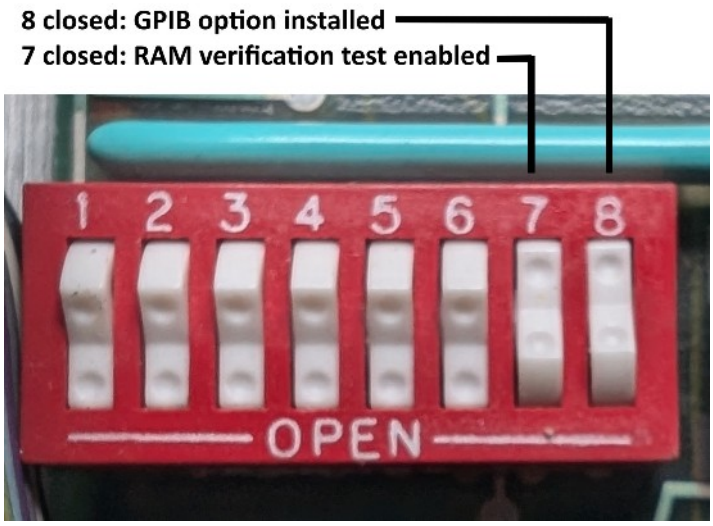


Using the standard Firmware ROM

To use the standard Firmware ROM functions, the jumper on the vintageTEK ROM board must be installed.

Section 7 of Service/Options Switch S707 (an eight-section DIP-switch assembly) on the top board (Storage Display Board) should be set to the closed position to enable the RAM Verification portion of the power-on self-test. If the scope is fitted with the GPIB option switch section 8 must be set to the closed position.

The settings of the other switches do not matter in normal mode.



Service / Options Switch S707 for normal operation

Using the Test/Diagnostic ROM.

To use the Test ROM functions, remove the Jumper “Firmware Selection” on the vintageTEK ROM board.

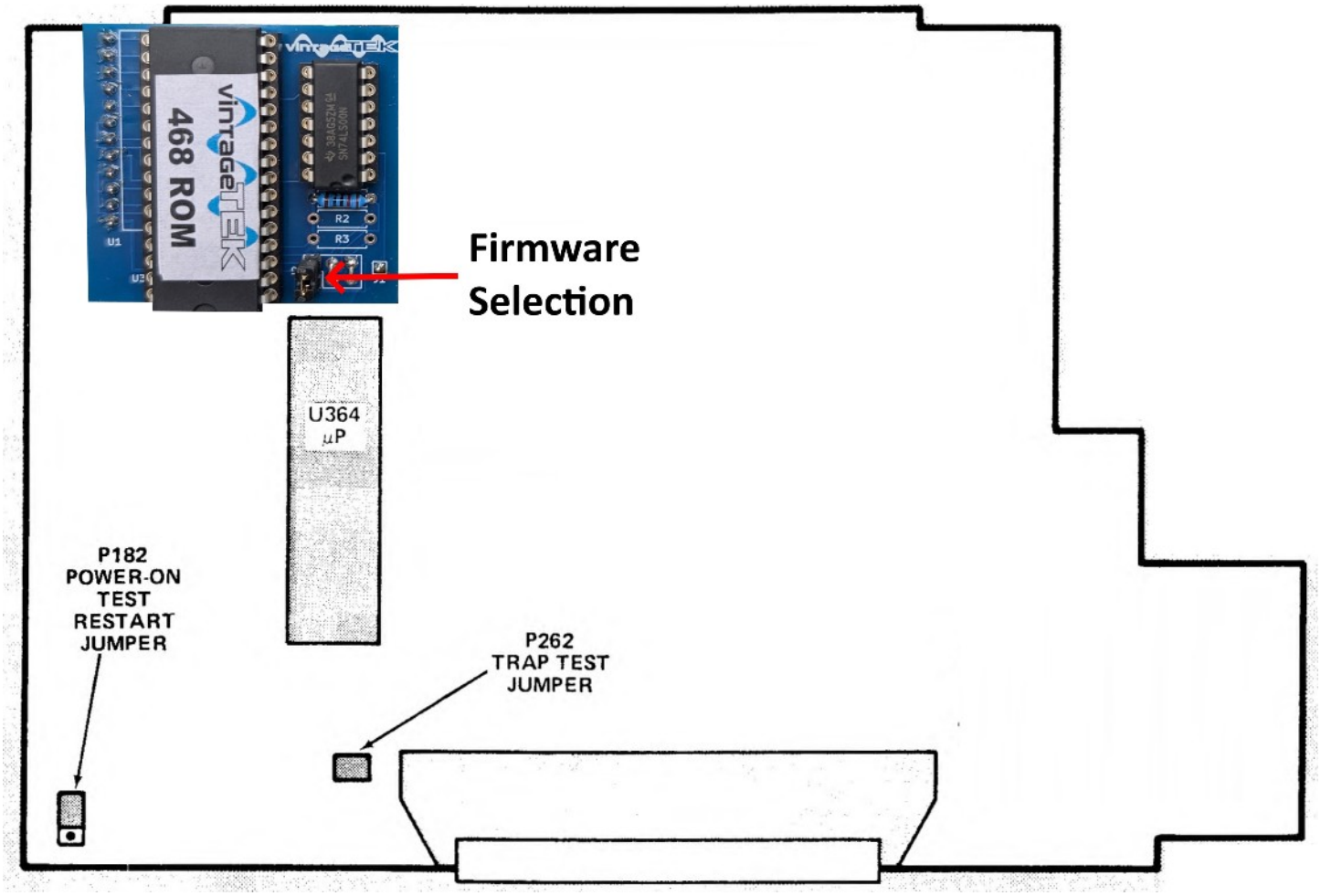


Figure 5-7. Location of the test ROM and test jumpers on the Microprocessor circuit board.

S707 on the Storage Display Board (top board)

Selecting a Service Routine

To select a specific service routine,set Service/Options switch S707 (an eight-section DIP-switch on the top board (Storage Display Board) to the number of the test desired. Table 5-4 lists the test routines and corresponding test numbers to be set into S707. Position 1, at the rear of the switch assembly, corresponds to the least-significant bit (LSB) of the test number. Position 8 is the Options-bit switch. If the GPIB option is not installed in the instrument, or when the GPIB option is not going to be used, switch 8 should be open. The GPIB service routines can be executed only when switch 8 is closed and the option installed. If you select a GPIB test, verify that the option bit is set to 1 (closed).

NOTE

When servicing of the instrument is completed, section 7 of Service/Options Switch S707 must be set to the closed position to enable the RAM Verification portion of the power-on self-test, and switch section 8 must be set to the closed position to enable the GPIB option.

Beginning a Service Routine

Once the service routine number has been set, power may be applied to the 468. The selected routine will begin to run in place of the normal power-on self-test. If the oscilloscope is already in operation, a routine can be started by removing Restart Jumper P182 from the RUN position and placing it momentarily in the RESTART position; then returning it to the RUN position. See Figure 5-7 for the location of the Restart Jumper on the Microprocessor circuit board.

Restarting a Service Routine

To restart a routine already in progress, remove Restart Jumper P182 from the RUN position and place it momentarily in the RESTART position; then return it to the RUN position. Cycling the POWER switch OFF then ON will also restart a service routine.

Table 5-4

Service Routine Switch Settings

Routine	Switch Setting
ROM Checksum	X0000000[a]
Lamp Test	X0000001
System and Scratch RAM Exercise	X0000010
I/O Registers	X0000011
Position-Rate Counter	X0000100
Switch Closure	X0000101
Basic Display System	X0001000
Stop at 256/Jitter Correction	X0001001
Stop at 512/Dot RAM	X0001010
Time Base Counter String (Signature Analysis Testing)	X0010000
Time Base Record String (Signature Analysis Testing)	X0010001
Time Base Jitter Counters (Signature Analysis Testing)	X0010010
Acquisition RAM	X0010011
GPIB Data Bus	11111000
Acceptor Handshake	11111001
Source Handshake	11111010
Default to 8888 display	Any other setting

[a]X in the switch setting column means "don't care." Either position of that switch selection is acceptable.

Selecting Another Routine

To select a different service routine, set the number of the desired new routine in the Service/Options switch and perform the service routine restart procedure. If the switch is inadvertently set to an invalid routine number, the seven-segment LED readout will display 8888. If you determine that the Service/Options DIP switch is set correctly but is not being read correctly, check the outputs of U522 (DIP Switch Register). The output of U522 is an inverted copy of the Service/Options switch setting.

SERVICE ROUTINE DESCRIPTIONS

ROM Checksum

This routine computes a checksum for the Service ROM. If the checksum computed by the routine is the same as the checksum stored in the ROM, the seven-segment display will read out all zeros. If there is a checksum failure, no display will appear and the Microprocessor will halt. If the checksum routine does not execute, oscilloscope operation is undefined.

Lamp Test

The lamp test routine will light each of the Microprocessor-controlled LED indicators on the instrument front panel (and the $\overline{\text{TIDS}}$/SRQ LED if the GPIB option is installed) in a predefined order. One LED at a time will be illuminated, and the test will continue until it is manually terminated. The order in which each LED illuminates is as follows:

1. Scaling: V/S, mV/ns, then DIV/μs.

2. The four digits of the seven-segment display will show a moving "8." from right to left (decimal points also illuminate).

3. CH 1 VOLTS/DIV Scale-factor: X1, then X10.

4. CH 2 VOLTS/DIV Scale-factor: X1, then X10.

5. $\overline{\text{TIDS}}$/SRQ: shows red then green.

NOTE

The red portion of the scaling LED will be illuminated when VOLTS CURSOR FUNCTION is selected and the green portion will be illuminated when the VOLTS CURSOR FUNCTION push button is released.

Position-Rate Counter

This routine exercises the Position-rate Counter circuitry. The contents of the counter (three binary-coded decimal characters) will be read and transferred directly to the seven-segment LED display. As the CURSOR control knob is rotated, the observed display should change. The range of the counter outputs should be within 000 to 800, with 80 being an average low-end count and 480 being an average high-end count. As the rate region of the control knob rotation is entered, the top scale-factor LED should illuminate. The bottom scale-factor LED should illuminate when the CURSOR SELECT push button is pressed in.

Switch Closure

This routine reads all of the Microprocessor-accessible switches and displays them in a logic analyzer type display. Four waveform displays will indicate the operation of 40 switches. The EXT trigger position of the SOURCE switch is not displayed, but it is indicated by illumination of the scale-factor LED when an external trigger is selected. See Figure 5-8 for an illustration of the waveform and the assigned area for each switch.

Each switch is assigned to one graticule division. A HI level means that the switch is closed, and a LO means that the switch is open. However, in the case of the AC-GND-DC switch, a three-level presentation is used to indicate all three possible switch positions. Switch operation can be checked by changing the switch position and observing the change seen on the display.

Basic Display System

No crt display is produced by this routine. A looping routine continually fills the Display RAM with a ramp to generate signatures. These signatures verify circuit operation when checked against the correct signatures contained in the Signature Tables. The following circuitry is exercised: display bus, counter addressing functions, Z-axis control circuitry used with the display bus, the Display RAM chip select circuitry, and the display address bus.

The vertical and horizontal digital-to-analog converters in the Storage Display circuitry will also be exercised, and their outputs may be checked with a test oscilloscope.

Stop at 256/Jitter Correction

This routine will fill the Display RAM with a 256-point waveform consisting of two ramps (see Figure 5-9A). The waveform data-point values range from 0 to 255 to obtain a display with both full vertical and full horizontal ranges. The jitter-correction circuitry is checked by selecting the X10 MAG function and using the Horizontal POSITION control to align the falling edge of the ramp with the center vertical graticule line. The waveform is cycled through the maximum value, the middle value, and the minimum value of the jitter correction, and the resulting display is three vertical lines. The lines should have a spacing of no more than 0.4 division between two adjacent lines, as illustrated in Figure 5-9B.

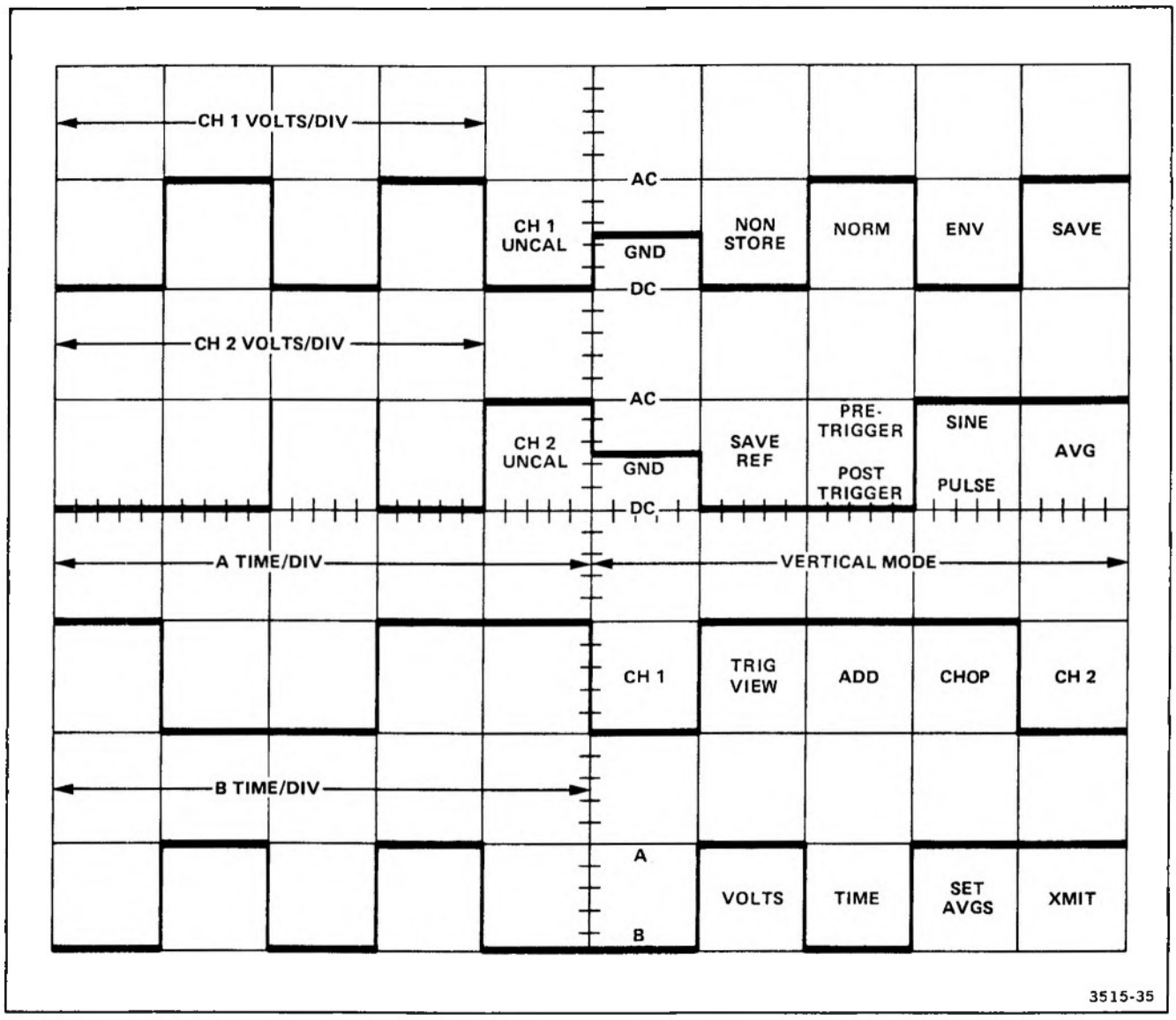


Figure 5-8. Switch closure test crt display.

Stop at 512/Dot RAM

This routine stores a 512-point waveform into the Display Memory. The display will consist of four 128-point ramps, with data-point values ranging from 65 to 190 (a five-division display). At the end of the waveform, four-point steps will appear. These steps have data-point values of 65, 128, and 190 respectively. The steps can be used to calibrate the vertical display gain by aligning the levels with both the dotted reference lines and the center horizontal graticule line (see Figure 5-10).

A dot display from the Dot RAM is moved through the ramp display to verify that a dot can be displayed on all 512 data points of the display.

Time Base Routine

The Time Base verification routines listed in Table 5-5 are used to generate signatures for signature-analysis testing. The portions of the Time Base circuitry not listed in the table cannot be controlled by the Microprocessor, and other troubleshooting methods are required (see "Troubleshooting Charts" in Volume II of this manual).

Acquisition RAM

This routine is used to generate signatures for testing the acquisition random-access memory. Data is written into each address in the RAM and then read back in a continuous loop routine. No crt display is generated by the routine.

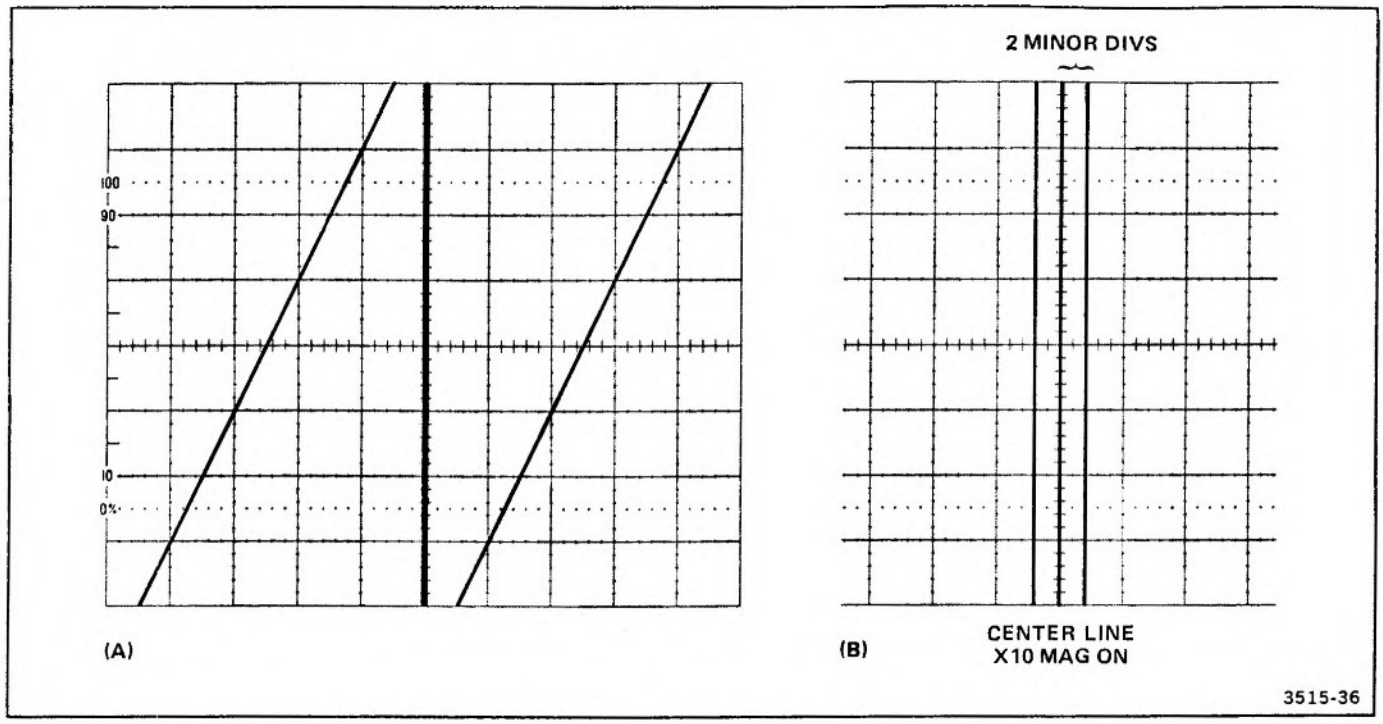


Figure 5-9. Stop at 256/jitter correction test crt display.

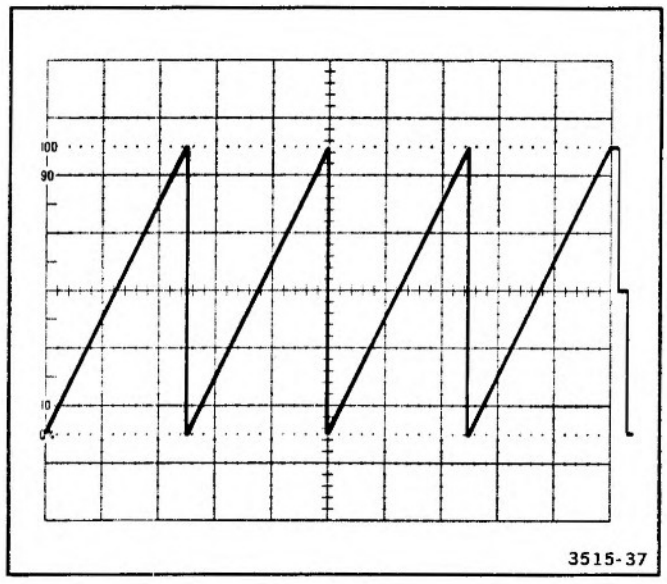


Figure 5-10. Stop at 512/dot RAM test crt display.

Table 5-5

Time Base Verification Routines

Test	Setup Requirements	Test Number
Time Base Counter String	Counter chain test jumper (P420) set to "Test" and triggers disabled.	X0010000
Time Base Record String	No additional requirements.	X0010001
Time Base Jitter Counters	No additional requirements.	X0010010

GPIB Data Bus

This routine toggles all the bits of the data path from the output data register through the bus bidirectional buffers and back to the Microprocessor bus through the data input buffer. The Microprocessor reads the Service/Options switch register and status buffer and compares the data against known values. The check value for the switch register must be manually set. The GPIB control register is also toggled, but only the TADS condition can be tested by the Microprocessor. The generated signatures can be checked by using signature-analysis testing to compare them with the Signature Tables.

Error codes are displayed in the seven-segment display and are updated at the completion of each pass through the routine. Table 5-6 shows the digit assignments and error indications.

To run the GPIB Data Bus routine, the following preliminary steup must be performed:

1. Disconnect the GPIB output cable.

2. Set the Service/Options switch to 111111000.

3. Set the GPIB switch talk address to 00000.

4. Set the TALK ONLY switch (switch-section 8) off (0).

Table 5-6

GPIB Data Bus Error Display

	Digit 1 Data Bus	Digit 2 Status Check	Digit 3 Switch Register	Digit 4 TADS
Pass	0	0	0	0
Fail	1-9	1-2	1	1-2

Acceptor Handshake

This rountine executes an acceptor handshake of the GPIB circuitry. Unused bits of the Interface Control register are used to drive the ATN and DAV lines, enabling the handshake to be executed. Signatures generated can be compared with the Signature Tables.

First perform the following preliminary setup:

1. Disconnect the GPIB output cable.

2. Set the Service/Options switch to 11111000.

3. Connect TP335 to TP112 on the GPIB board to drive ATN.

4. Connect TP333 to TP114 on the GPIB board to drive DAV.

Source Handshake

In this routine, a source handshake loop is executed and the bits of the Interface Status register are tested by the Microprocessor. Errors are displayed in the seven-segment display. Generated signatures can be compared with the Signature Tables. A jumper is needed to assert DAC, and RFD is always True to enable the handshake routine.

First perform the following preliminary setup:

1. Disconnect the GPIB output cable.

2. Set the Service/Options switch to 11111010.

3. Connect TP335 to TP111 on the GPIB board to assert DAC.

4. Connect TP333 to TP113 on the GPIB board to assert IFC.

If no errors occur during execution of the routine, the readout in the seven-segment display will be 0000. If a status-bit error occurs, a number from 1 through 7 will appear in the LSB of the readout. The remaining digits are not used.